NAVAL POSTGRADUATE SCHOOL
Monterey, California

THESIS

THE DESIGN OF THE RADIO FREQUENCY (RF) SUBSYSTEM PRINTED CIRCUIT BOARDS FOR THE PETITE AMATEUR NAVY SATELLITE (PANSAT)

by

Carl Andrew Lahti

June, 1997

Thesis Advisor: Randy L. Borchardt
Co-Advisor: Rudolf Panholzer

Approved for public release; distribution is unlimited

REPORT DOCUMENTATION PAGE

Form Approved OMB No. 0704-0188

1. AGENCY USE ONLY *(Leave blank)*	2. REPORT DATE June 1997.	3. REPORT TYPE AND DATES COVERED Engineer's/Master's Thesis

4. TITLE AND SUBTITLE The Design of the Radio Frequency (RF) Subsystem Printed Circuit Boards for the Petite Amateur Navy Satellite (PANSAT)

5. FUNDING NUMBERS

6. AUTHOR(S) Lahti, Carl A.

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
Naval Postgraduate School
Monterey CA 93943-5000

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

10. SPONSORING/MONITORING AGENCY REPORT NUMBER

11. SUPPLEMENTARY NOTES The views expressed in this thesis are those of the author and do not reflect the official policy or position of the Department of Defense or the U.S. Government.

12a. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release; distribution is unlimited.

12b. DISTRIBUTION CODE

13. ABSTRACT *(maximum 200 words)*

The Petite Amateur Navy Satellite (PANSAT) is a small digital communication satellite being developed by the Space Systems Academic Group and the Naval Postgraduate School. This thesis describes the layout of the three final flight printed circuit boards for the radio frequency (RF) subsystem for PANSAT. The circuits and layouts are documented in detail. A link analysis is performed to verify system design and a power budget provided for integration with other satellite systems. Printed circuit board design fundamentals and high frequency printed circuit board construction techniques are also described.

14. SUBJECT TERMS
Printed Circuit Board, Low Earth Orbit Satellite, RF Communications

15. NUMBER OF PAGES 110

16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
Unclassified	Unclassified	Unclassified	UL

NSN 7540-01-280-5500

Standard Form 298 (Rev. 2-89)
Prescribed by ANSI Std. 239-18 298-102

Approved for public release; distribution is unlimited.

THE DESIGN OF THE RADIO FREQUENCY (RF) SUBSYSTEM PRINTED CIRCUIT BOARDS FOR THE PETITE AMATEUR NAVY SATELLITE (PANSAT)

Carl Andrew Lahti
Lieutenant, United States Navy
B.S.S.E., United States Naval Academy, 1989

Submitted in partial fulfillment
of the requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING
and
ELECTRICAL ENGINEER

from the

NAVAL POSTGRADUATE SCHOOL
June 1997

Author: _____
Carl A. Lahti

Approved by: _____
Randy L. Borchardt, Thesis Advisor

_____
Rudolf Panholzer, Co-Advisor

_____
Herschel H. Loomis, Jr., Chairman
Department of Electrical and Computer Engineering

ABSTRACT

The Petite Amateur Navy Satellite (PANSAT) is a small digital communication satellite being developed by the Space Systems Academic Group and the Naval Postgraduate School. This thesis describes the layout of the three final flight printed circuit boards for the radio frequency (RF) subsystem for PANSAT. The circuits and layouts are documented in detail. A link analysis is performed to verify system design and a power budget provided for integration with other satellite systems. Printed circuit board design fundamentals and high frequency printed circuit board construction techniques are also described.

TABLE OF CONTENTS

I. INTRODUCTION

A. SATELLITE COMMUNICATIONS

A satellite communications system consists of a satellite in space linking multiple ground stations on the earth. Modulated RF waveforms, either analog or digital, represent the information in the system. Satellite communications systems are "line of sight" due to their high operating frequencies. Signals at these high frequencies travel in a straight line and the antenna on the satellite must physically have an uninterrupted line of sight to the ground station antenna. In analog satellite communications, the satellite typically acts as a space based reflector. The satellite receives an analog transmission from a ground station, amplifies and retransmits the signal for receipt by all ground stations within the satellite footprint. In digital satellite communications, the satellite may act as a "dumb" space based reflector as in analog communications or it may be a regenerative repeater. Regenerative repeaters contain processing equipment to demodulate the incoming waveform, process the information and retransmit the processed information. Typically this processing involves error correction.

Satellites exist in different orbits around the earth. The satellites farthest from the earth are in geostationary orbit at a height of 35786 km above the surface of the earth and an inclination of 0 degrees. These satellites orbit the earth at the same rate the earth is spinning about its axis, thus appearing stationary to an observer on the earth. Geostationary satellites, with their great height, provide a large footprint where multiple ground stations can access the same satellite at the same time.

Low earth orbit (LEO) satellites orbit the earth at heights from 300 km to 1500 km. A LEO satellite has a much smaller footprint than the geostationary satellite. A given ground station may only be able to access the LEO satellite for several minutes each day as its footprint passes over the ground station. LEO satellites require significantly less transmitted power than geostationary satellites because the distance between the satellite and ground station is significantly less and the corresponding energy loss is less.

The RF subsystem of a satellite processes RF waveforms. It typically receives a signal from the satellite's antenna, filters and amplifies the signal and converts its frequency to a lower intermediate frequency (IF) for further processing and demodulation. The subsystem also receives a signal for transmission at the IF and converts it to the RF transmission frequency, then amplifies the signal and sends it to the antenna for transmission.

B. PANSAT

The Petite Amateur Navy Satellite (PANSAT) is a small, LEO satellite being designed by the Space Systems Academic Group at the Naval Postgraduate School in Monterey, California. PANSAT will provide store and forward communications to users in the 70 cm amateur radio band. The satellite will act as an orbital server with 4 MB of storage using the AX.25 packet protocol. When the user is in the satellite footprint he may log onto the satellite's computer and check for any files addressed to him. He may also upload files for other users. The satellite will transmit and receive at a center frequency of 436.5 MHz using direct sequence spread spectrum (DSSS), differentially encoded phase shift keying (DPSK) modulation. The communications data rate will be

second with a chipping rate of 1.25 mega chips per second. The chipping sequence is a pseudo random noise sequence produced from a 7 stage linear feedback shift register. The satellite will also have a narrow band high data rate channel with a data rate of 78125 bits per second. Use of the high data rate channel is privileged and intended for ground controllers at the Naval Postgraduate School for maintenance and software upgrades. PANSAT, shown with approximate dimensions in Figure 1, is planned for launch in late 1997 from the space shuttle through the hitchhiker program. Launch during a MIR space station rendezvous mission, could place the spacecraft at an inclination of at least 28 degrees. The technical specifications for PANSAT are documented in the required filing to the International Telecommunication Union [Ref.1].

C. PROJECT OVERVIEW

This thesis serves to document the design of the printed circuit boards in the RF subsystem for PANSAT. It incorporates a detailed link budget analysis to verify system design meets the required specifications. The electrical and physical designs are described in detail. The basic process of printed circuit board design and stripline circuit construction are described in appendices.

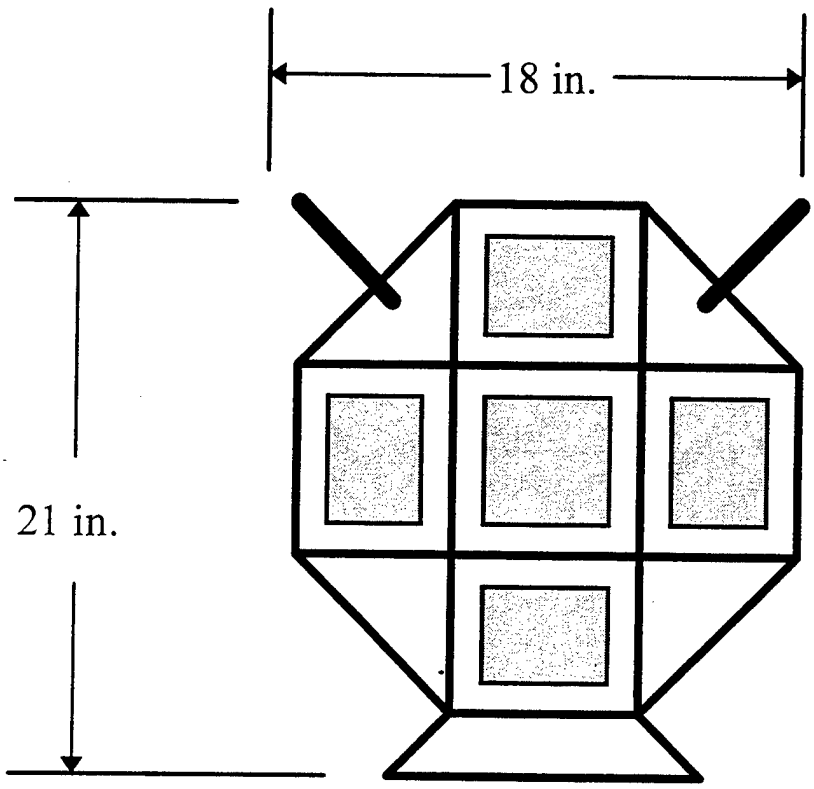


Figure 1 PANSAT - Side View.

II. BACKGROUND

A. PANSAT SYSTEMS LAYOUT

The electronics in the satellite consists of the following major subsystems in addition to the RF subsystem: electrical power (EPS), digital control (DCS), mass storage, temperature monitoring (TMUX). These systems work together to provide the functionality of the satellite operating under the control of the satellite's system controller. A wiring harness containing power and control signals connects the subsystems. Figure 2 shows the basic layout of the subsystems.

The EPS controls the charging of the batteries via the solar cells and the distribution of power to the rest of the spacecraft. The satellite has 18 solar panels for the production of power. Two banks of 9 batteries each store power. Each battery bank has the capability of providing complete power for the satellite. The DCS commands the EPS to provide power to the subsystems of the satellite.

The digital control subsystem is the computer that provides control for all functions of the satellite. The digital control subsystem has two completely separate, redundant systems. The subsystem consists of the modem and the control microprocessor. The heart of the modem is the PARAMAX PA-100 spread spectrum demodulator functioning under direct control of the DCS microprocessor. The control processor is an Intel 80186 processor. The DCS controls all satellite functions.

The mass storage system provides the memory needed for storage of the files uploaded to the satellite by users of the satellite. It contains two redundant systems, each

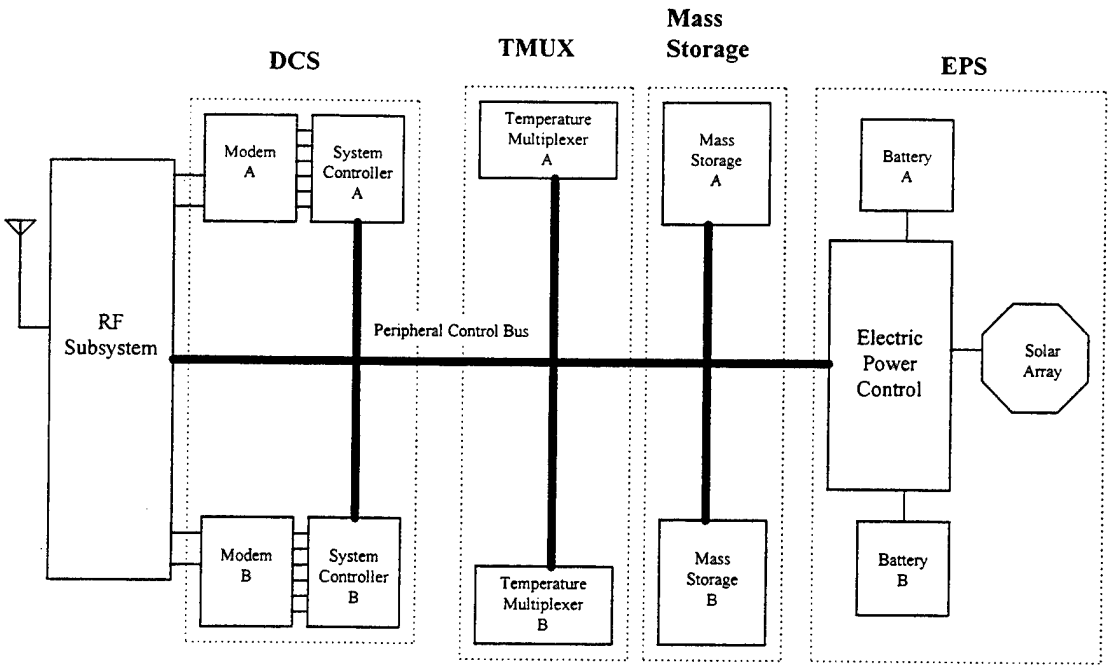


Figure 2 PANSAT System Diagram

with 4 mega bytes of random access memory. The memory is self error correcting to correct any potential errors in data coming from single event upsets induced by space radiation.

The TMUX is an analog multiplexer that directs which temperature sensor is being read by the DCS. There are temperature sensors on all major satellite components to provide a monitoring capability. The DCS will periodically read the temperature on various components and record the data in the mass storage system for later down loading by the satellite's operators.

B. RF SUBSYSTEM DESIGN BACKGROUND

Brown [Ref.2] performed initial design work for the PANSAT RF subsystem. Brown's work was the initial design for the PANSAT communications system. Brown designed a binary phase shift keyed direct sequence spread spectrum using parameters established during a preliminary link analysis. His work included a complete modem and RF system design as well as printed circuit board (PCB) layouts. Brown's design became obsolete when the modem became based around the PARAMAX PA-100 spread spectrum demodulator integrated circuit.

Building upon Brown's work, Dawson and Eagle [Ref.3] conducted a redesign of the RF subsystem. Their design goal was to reconfigure the system so any one lost low-noise amplifier (LNA), and high-power amplifier (HPA), and oscillator would still allow the use of either DCS. They also identified specific components for use and constructed a partial working model using connectorized components, and obtained test data from the model. Figure 3, less the bandpass filters on the IF side of the mixer, was the design produced by Dawson and Eagle.

Figure 3 shows block diagram of the RF subsystem. The flight version of this system consists of three separate PCB's, a RF switching PCB, a RF LNA PCB and a RF HPA PCB. An additional PCB serves as an interface between the peripheral control bus and the RF subsystem, providing control and power to the system. A staff engineer at the Space Systems Academic Group of the Naval Postgraduate School designed the interface of the RF subsystem with the DCS as well as the PCB for the interface.

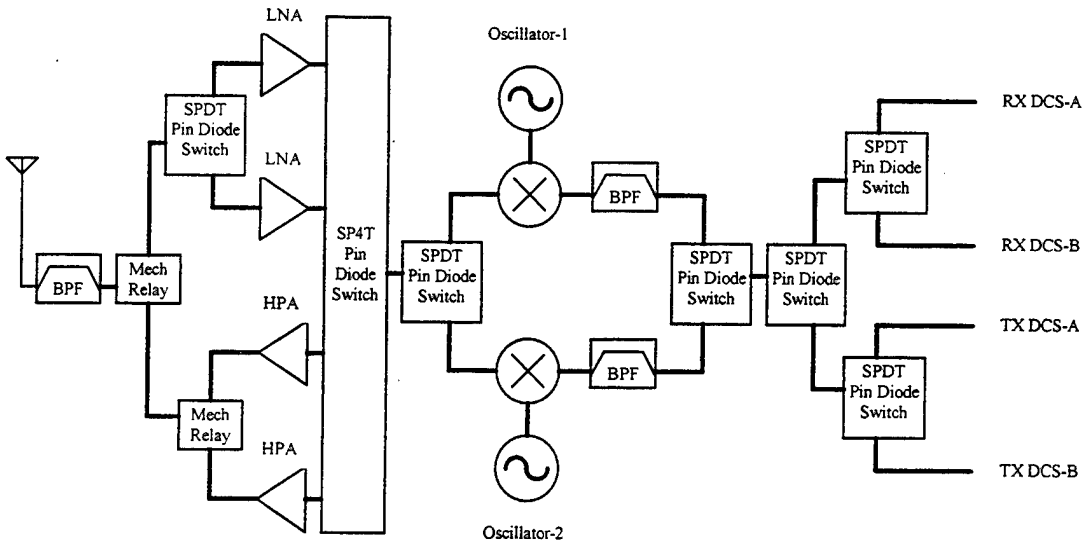


Figure 3 RF subsystem Block Diagram

Gericke [Ref.4] designed the housing for the RF subsystem. Figure 4 shows the RF subsystem housing. The unusual shape allows the subsystem to fit within the constraints of the spacecraft. The 4 pockets in the housing provide mounting areas for the Switching, HPA, LNA and power and control interface PCB. A top cover fits over all the pockets in the housing and provides protection and EMI shielding.

The circuit boards are designed using an exterior geometry to fit within the housing designed by Gericke [Ref.4]. A sophisticated computer aided design tool produced by Cadence Design Systems was used for the circuit board layout. Design rules for high frequency PCB construction from several sources were used to assure signal integrity. The following chapter describes the circuit and PCB designs in detail.

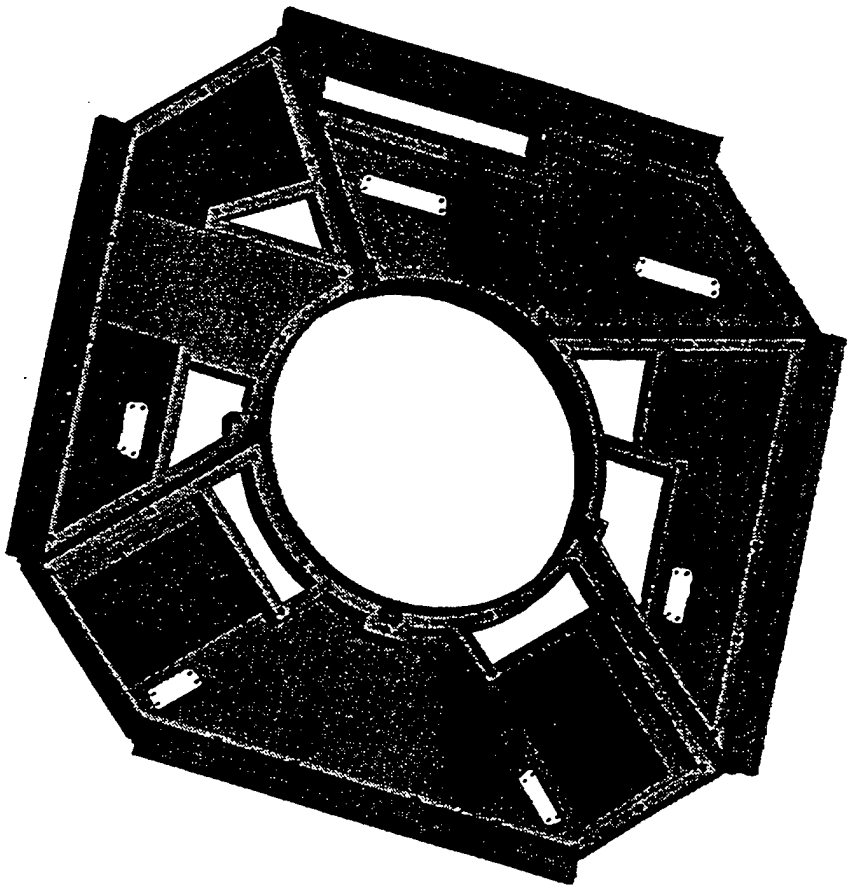


Figure 4 RF Housing. From Ref.[4].

III. RF SUBSYSTEM PRINTED CIRCUIT BOARD DESIGN

A. PRINTED CIRCUIT BOARD EXTERIOR GEOMETRY

The RF subsystem PCB design was accomplished using electronic computer aided design tools created by Cadence Design Systems including the Concept schematic capture tool and the Allegro PCB layout tool. The unusual exterior geometry of the PCB's required special care in design.

The housing for the RF subsystem was designed using the IDEAS computer aided design software from the Structural Design Research Corporation. The housing was manufactured at the Naval Postgraduate School using a numerically controlled milling machine. The control data for the milling machine came form the IDEAS drawings. The aerospace engineer designing the housing created mechanical drawings of the RF subsystem PCB's using IDEAS. These outlines mirrored the inside of the housing's PCB pockets, shrunk by 1/32" in all exterior dimensions. The holes, connector locations and mounting surfaces were then added to the PCB drawing. This produced a three dimensional PCB model which fit exactly into the housing.

These drawings were then electronically imported into the Allegro layout program, where they became the PCB outline and references for mounting hole placement. This allowed precise control of the physical dimensions of the PCB's without the tedious, error prone process of transcribing data from conventional drawings.

The completed PCB drawings from Allegro were then exported to the IDEAS program where they became three dimensional models. The components appeared as

boxes on the surface of the PCB. The PCB was then checked for fit into the housing prior to manufacture, ensuring a precise fit and eliminating the need for redesign due to a physical size mismatch.

B. RF SWITCHING PRINTED CIRCUIT BOARD

1. Functional Description

The switching section serves to up convert the outgoing IF from the DCS to RF and route the signal to the desired LNA. It also receives the incoming RF from the selected HPA and down-converts the signal to IF, routing the signal to the desired DCS. Figure 5 contains a block diagram of the RF switching PCB. Appendix A contains detailed schematic diagrams of the RF switching PCB.

A transistor-transistor logic (TTL) level input on each individual switch controls

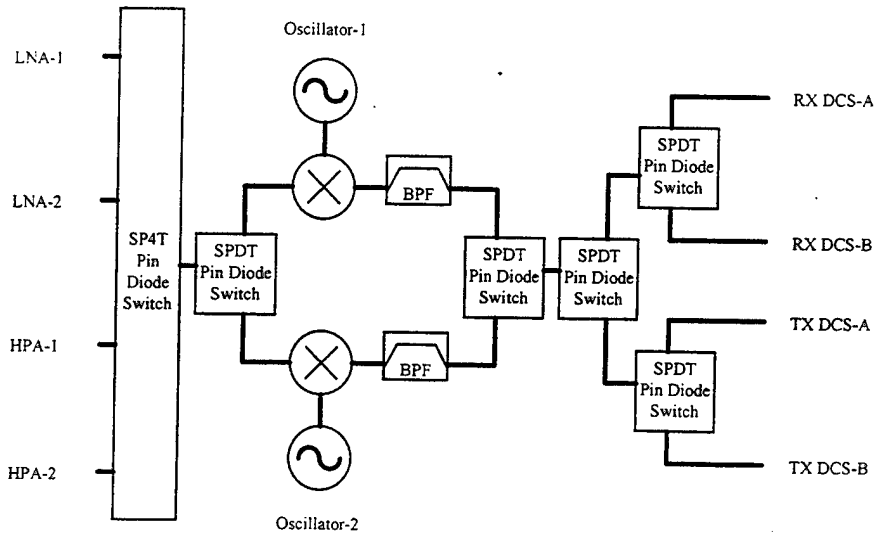


Figure 5 RF Switch PCB Block Diagram

the positions of the pin diode switches. Figure 6 shows the numbering scheme used for the TTL switch inputs. A 54HC245 integrated circuit, located on the RF switching PCB, buffers the TTL inputs to the RF switching PCB. This buffering assures a sufficient signal level present at the TTL input to the switches to prevent spurious switching caused by noise on the wiring harness coming into the RF switching PCB.

The network is half duplex, meaning that either transmission or reception can occur, but not both at the same time. The switching network is capable of selecting any combination of amplifier, oscillator and system controller. This grants fault tolerance by allowing any amplifier, and any oscillator and any system controller to fail simultaneously, while still allowing the system to function without a loss of performance.

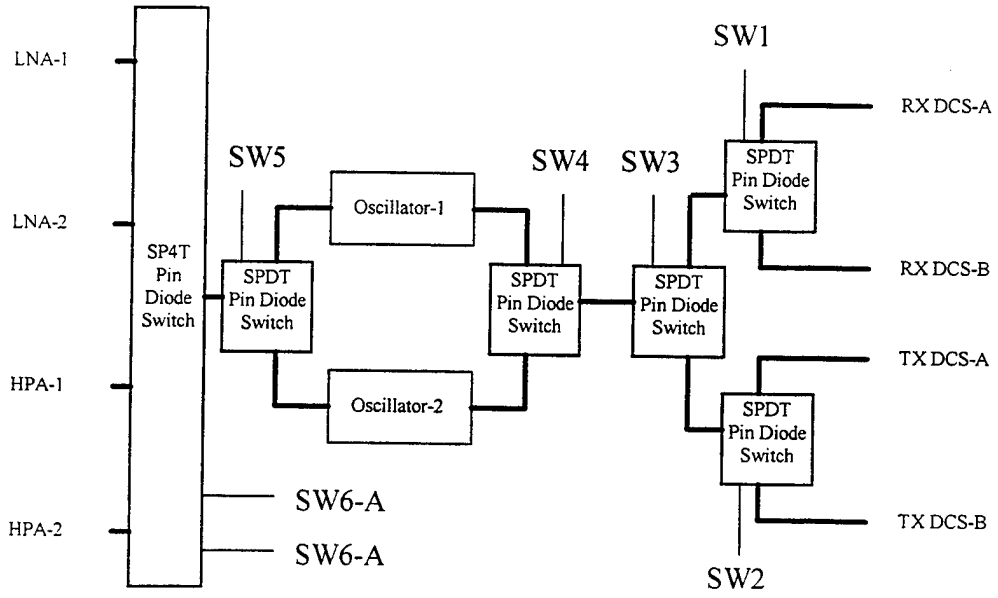


Figure 6 RF Switching network TTL inputs

For both transmitting and receiving, primary paths have been designated, based on the active DCS. These primary paths will be the default switch positions selected by the RF control board, based on the control board sensing the active DCS. Table 1 shows all possible states of the RF switching system, including the primary paths for each DCS. The non-primary paths allow the DCS to choose an alternate signal path, should the primary path be inoperative or the DCS desire to exercise other components. Table 1 also lists the TTL inputs required on the signal lines to achieve the desired switch positions.

All the pin diode switches receive power from the same +5 VDC power input to the RF switching PCB. Whenever the RF subsystem is powered on, the switches must have power continuously to assure they are in the desired state. This justifies the use of a

Designation	Path	SW1	SW2	SW3	SW4	SW5	SW6-A	SW6-B
Primary Rx DCS-A	LNA-1,OSC-1,DCS-A	0	X	0	0	1	1	0
	LNA-1,OSC-1,DCS-B	1	X	0	0	1	1	0
	LNA-1,OSC-2,DCS-A	0	X	0	1	0	1	0
	LNA-1,OSC-2,DCS-B	1	X	0	1	0	1	0
	LNA-2,OSC-1,DCS-A	0	X	0	0	1	1	1
	LNA-2,OSC-1,DCS-B	1	X	0	0	1	1	1
	LNA-2,OSC-2,DCS-A	0	X	0	1	0	1	1
Primary Rx DCS-B	LNA-2,OSC-2,DCS-B	1	X	0	1	0	1	1
Primary Tx DCS-A	HPA-1,OSC-1,DCS-A	X	0	1	0	1	0	1
	HPA-1,OSC-1,DCS-B	X	1	1	0	1	0	1
	HPA-1,OSC-2,DCS-A	X	0	1	1	0	0	1
	HPA-1,OSC-2,DCS-B	X	1	1	1	0	0	1
	HPA-2,OSC-1,DCS-A	X	0	1	0	1	0	0
	HPA-2,OSC-1,DCS-B	X	1	1	0	1	0	0
	HPA-2,OSC-2,DCS-A	X	0	1	1	0	0	0
Primary Tx DCS-B	HPA-2,OSC-2,DCS-B	X	1	1	1	0	0	0
"0"=TTL Low "1"=TTL High "X"=don't care								

Table 1 RF Switching Paths

common power supply for all the switches, as they could not operate independently and maintain system functionality. The +5 VDC switch power supply also supplies power to the 5HC245.

Each oscillator has a separate +12.5 VDC power supply input to the RF switching PCB. This allows individual control of each oscillator. The EPS, through the RF control PCB and under command from the DCS, supplies all power to the RF subsystem.

The RF switching board provides locations for two temperature sensors. One temperature sensor is physically located near each oscillator. The oscillators have the largest power consumption and will produce the most heat on this PCB. The temperature sensors, under control of the TMUX, will monitor this temperature.

The RF switching PCB uses SMA connectors and coaxial cables to route IF and RF signals into and out from the board. The IF connection to and from the DCS is made through the equipment plate of the satellite to SMA connectors mounted on the top of the PCB. The RF connections to the HPA and LNA sections are made through the bottom of the RF housing from SMA connectors mounted on the bottom of the PCB.

The board also contains two 15 pin connectors that supply power and control signals to the board as well as the signals from the temperature sensors located on the board. Table 2 and Table 3 show the pin connections for the 15 pin connectors. Capture screws secure the RF switching PCB into its housing. This places the bottom of the PCB in intimate contact with the housing.

Pin Number	Function
1	+12 Volts (OSC #1)
2	SW6-A
3	SW6-B
4	SW5
5	SW4
6	SW1
7	SW3
8	SW2
9	Ground
10	Ground
11	Ground
12	Ground
13	Ground
14	Temp Sensor A
15	Temp Sensor B

Table 2 Connector #1 Pin Description

Pin Number	Function
1	Ground
2	Ground
3	Ground
4	Ground
5	Ground
6	Ground
7	Ground
8	+5 V DC
9	Temp Sensor A
10	Ground
11	Temp Sensor B
12	Ground
13	+12 V DC (OSC #2)
14	Ground
15	Ground

Table 3 Connector #2 Pin Descriptions

2. Circuit Description

The circuit to accomplish frequency conversion is a simple heterodyning circuit consisting of an oscillator and a mixer. The RF carrier frequency (f_C) is 436.5 MHz and the IF (f_{IF}) is 70 MHz. The oscillator frequency (f_{LO}) is set at 366.5 MHz. The switching circuit provides no amplification, allowing any radiated noise associated with the frequency conversion to stay within the housing for the RF switching PCB. This also simplifies PCB layout and power requirements.

During the receive operation, the oscillator output to the IF stage will be $f_C \pm f_{LO} = \begin{matrix} 436.5 + 366.5 = 803 & MHz \\ 436.5 - 366.5 = 70 & MHz \end{matrix}$. The band pass filters on the IF side of the mixers provide for rejection of the 803 MHz signal, providing in excess of 40 dB attenuation. The desired RF input frequency to the oscillator is $f_{LO} + f_{IF}$, 436.5 MHz. If the input frequency is $f_{LO} - f_{IF} = 366.5 - 70 = 296.5 \quad MHz$, the image frequency, the oscillator will also produce the 70 MHz IF signal. This will result in the simultaneous reception of signals at two different carrier frequencies. The RF section of the receiver removes the image frequency. The band pass filter at the input to the RF section serves as an image rejection filter, attenuating the image frequency.

During the transmit operation, the oscillator output to the RF will be $f_{LO} \pm f_{IF} = \begin{matrix} 366.5 + 70 = 436.5 & MHz \\ 366.5 - 70 = 296.5 & MHz \end{matrix}$. The frequency selectivity of the HPA and the band pass filter at the output of the RF section attenuate the unwanted 296.5 MHz frequency. The modem up-converts the 10 MHz in the PA-100 demodulator to the 70

MHz IF. The band pass filters on the IF side of the mixers now serve to attenuate any unwanted frequencies from the conversion in the modem.

Table 4 lists the signal losses for the components on the RF switching PCB. The total loss is 12.5 dB. This assumes the oscillator is producing +7 dBm output power. The transmission lines in the modem and amplifiers are matched to a 50 Ω impedance, as are internal mixer input and output. This necessitates matching the IF and RF signal paths to a 50 Ω impedance to minimize return loss.

3. Power Requirements

The power supplies for the switches and oscillators are regulated outside the circuit. The power is filtered immediately after it is launched onto the RF switching PCB. This provides protection for the components from spikes in the power supply and reduces emitted electromagnetic radiation. A series of capacitors short the DC power input lines to ground, reducing the effect of power spikes. The input power is coupled through a ferrite core bead to reduce EMI. This filtering prevents any noise on the power supply from reaching the integrated circuits and any noise generated on the PCB from getting back into the power supplies. The oscillators and switches receive their power through a

Component	Loss
SPDT Pin Diode Switch	1.3 dB
SP4T Pin Diode Switch	1.1 dB
PIF-70 Band Pass Filter	1.1 dB
Mixer	5.1 dB (conversion loss)

Table 4 RF Switching PCB Signal Losses

power plane. This provides a low inductance, high-frequency distributed capacitance that further reduces power supply noise and eliminates the need to locate a capacitor next to each of the switches.

Table 5 lists the components on the RF switching board and their power requirements. The total power required for the RF switching PCB operation is 950 mW. This assumes that both oscillators are turned on simultaneously.

4. PCB Layout

The RF switching PCB consists of 6 signal layers separated by FR-4. Detailed drawings and photoplots are contained in Appendix A. Figure 7 shows the layer by layer buildup of the RF switching PCB. The bottom 3 layers of the RF switching PCB form a stripline structure for high frequency transmission lines. Appendix E discuses stripline circuit construction. The bottom layer and the ground layers are identical. The power layer provides power to all components and the top layer routes control signals.

Component	Quantity	Voltage Supply	Current Required (ea)	Power Required (total)
SDPT Pin Diode Switch	5	+5 VDC	10 mA	250 mW
SP4T Pin Diode Switch	1	+5 VDC	10 mA	50 mW
366.5 MHz Oscillator	2	+12.5 VDC	20 mA	500 mW
TTL Buffer	1	+5 VDC	5 mA	25 mW

Table 5 RF Switching Circuit Components

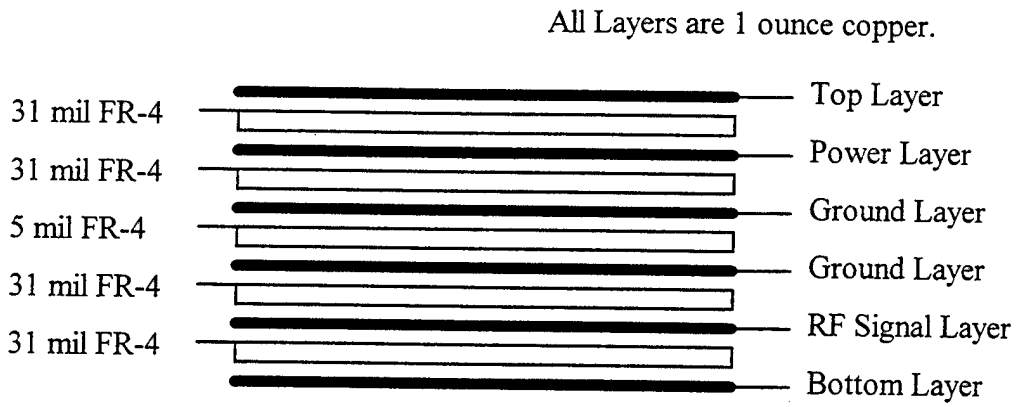


Figure 7 RF Switching PCB Cross Section

The RF switching PCB contains 2 ground planes in the center. The lower one provides the top of the stripline structure. The upper one creates an even number of layers in the PCB. This helps in the manufacturing process to prevent the PCB from warping as the layers are roll bonded together.

The top layer contains surface mount components for power filtering and control signal routing. Surface mount components are small and require no holes drilled through the PCB for mounting. The plane areas on the top layer surround the SMA connectors serving as the interface with the DCS. These plane areas, at ground, are placed there because the lip of an opening in the lid of the housing comes into contact with the surface of the PCB. This allows the housing to remain "RF tight," provides shielding for the PCB, and makes an easy structure to assemble.

The power layer contains 3 separate planes supplying power to the switches, the oscillators and the 54HC245 buffer. The power is routed, from the connectors, through a

filtering network on the top layer. From the filtering network, vias provide the connection with the power planes. The left and right planes in Figure 24 supply individual power to each oscillator. The center plane supplies power to all the switches and the 54HC245 integrated circuit.

The RF signal layer routes RF and IF between components. It requires a critical geometry, as discussed in Appendix E. The trace width for a 50 Ω characteristic impedance is calculated below using Equation (2) and Equation(3); with t = 1.4 mil, b = 31 mil, and ε_R=4.6, the relative dielectric constant for FR-4.:

$$C_f' = \frac{0.0885(4.6)}{\pi}\left[\frac{2}{1-\frac{1.4}{31}}\ln\left(\frac{1}{\left(1-\frac{1.4}{31}\right)}+1\right)-\left(\frac{1}{1-\frac{1.4}{31}}-1\right)\ln\left(\frac{1}{\left(1-\frac{1.4}{31}\right)^2}-1\right)\right]$$

$$= 0.19601\ pf\ /\ cm$$

$$w = 31\left(\frac{94.15}{50\sqrt{4.6}}-\frac{0.19601}{0.0885(4.6)}\right)\left(1-\frac{1.4}{31}\right) = 24.026\ mil$$

The components mounted on the bottom handle the RF signal processing. They are in hermetically sealed metal cans mounted in contact with the bottom ground plane. The bottom layer also serves as a mounting point for the SMA connectors going to the HPA and LNA sections. The PCB bottom, in the area surrounding the SMA connectors, is mounted against flanges in the bottom of the housing which provide an "RF tight" enclosure.

B. RF LNA PRINTED CIRCUIT BOARD

1. Functional Description

The RF LNA board is used to provide the first amplification of the signal after the antenna. Figure 8 shows a block diagram of the LNA section. It receives the signal from the antenna and sends it to one of two duplicate low noise amplifiers. Table 6 shows the states of the pin diode switch and the required TTL inputs. After amplification, the signal is sent to the RF switching PCB for frequency down conversion and routing to the DCS. A detailed schematic of the LNA circuit is provided in Appendix B.

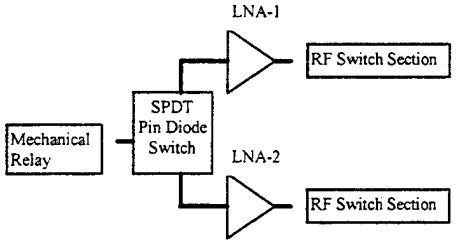


Figure 8 RF LNA PCB Block Diagram

LNA Selection	Switch TLL Input
LNA-1	0
LNA-2	1

Table 6 RF LNA PCB Switch States

The RF LNA PCB requires +5 VDC power for each LNA, +5 VDC for the pin diode switch and +5 VDC for the 54HC245 buffer. The power supply for the pin diode switch and the 54HC245 are combined. Two temperature sensors are provided as in the RF switching PCB. Table 7 shows the connector pin assignment for the RF LNA PCB.

2. Circuit Description

The low noise amplifiers used in the circuit are Avantec UTC-554. They have a minimum gain of 28 dB with a maximum noise figure of 3.0 dB. Each LNA is placed between an SMA connector and the pin diode switch. Each LNA has a separate power connection in the 15 pin connector allowing individual control of the power to each LNA. The power is filtered through a capacitor network and ferrite bead on lead as in the RF

Pin Number	Function
1	+5 VDC LNA-1
2	Ground
3	+5 VDC LNA-2
4	Ground
5	+5 VDC Pin Diode Switch
6	Ground
7	Ground
8	Ground
9	Temp Sensor A-1
10	Ground
11	Temp Sensor A-2
12	Ground
13	Temp Sensor B-1
14	Temp Sensor B-2
15	TTL Switch Control

Table 7 RF LNA PCB Connector Pin Assignments

switching PCB.

The control signal for the switch is also passed through a 54HC245 buffer as in the RE switching PCB. The loss through the pin diode switch is 1.1 dB. This yields a total gain for the LNA PCB of 26.9 dB.

3. Power Requirements

Each LNA requires 40 mA at +5 VDC for a total power of 200 mW each. The pin diode switch required 50 mW and the 54HC245 requires 20 mW. This yields a total RF LNA PCB power requirement of 470 mW if both low noise amplifiers are operating at the same time.

4. PCB Layout

The RF LNA PCB is composed of 4 layers with an FR-4 dielectric between the layers. It uses stripline circuit construction as in the RF switching PCB. Appendix B contains the detailed photoplot and assembly drawings for the RF LNA PCB. Figure 9 shows a cross section of the RF LNA PCB.

The stripline circuit geometry for the LNA PCB is identical to the geometry for the Switching PCB. This means the 50 Ohm characteristic impedance trace width is the same as in the switching PCB. This layout was completed without the use of power planes to minimize PCB complexity and reduce manufacturing costs. Additional power supply filtering and wide traces are used for the power supply connections to minimize the impact of not using power planes.

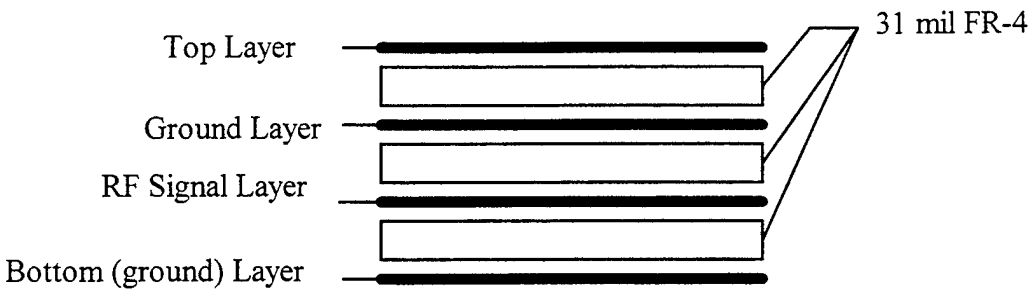


Figure 9 RF LNA PCB Cross Section

C. RF HIGH POWER AMPLIFIER PRINTED CIRCUIT BOARD

1. Functional Description

The HPA PCB serves to amplify outgoing transmission to the required level to ensure successful data link closure. Figure 10 shows a block diagram of the RF HPA PCB. The HPA string contains 2 amplifiers, a preamp to boost the signal to approximately 0 dBm and the final power driver stage. Detailed schematic drawings are contained in Appendix C.

The final output amplifier has an output of 5W. This power level prohibited the use of a pin diode switch for selecting the HPA output for the antenna. A mechanical relay is used. This also improves the isolation between HPA stages by 30 dB over a pin diode switch. Due to the high gain and power required by the HPA sections, only one may have power applied at any given time. Table 8 lists the pin connections for the connector on the RF HPA PCB.

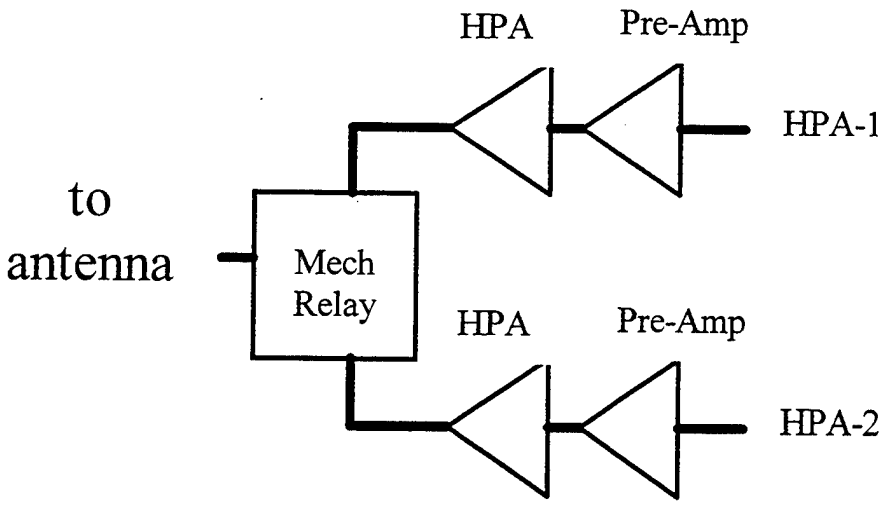


Figure 10 RF HPA PCB Block Diagram

Pin Number	Function
1	Temp Sensor A-1
2	Temp Sensor A-2
3	Temp Sensor B-1
4	Temp Sensor B-2
5	+5 VDC HPA-2 Pre Amp
6	0 to +5 VDC HPA-2 Control
7	Ground
8	+6 VDC HPA-2 Power
9	+5 VDC HPA-1 Power
10	Ground
11	+5 VDC Relay Coil Power
12	0 to +5 VDC HPA-1 Control
13	Ground
14	Ground
15	+6 VDC HPA-1 Power

Table 8 RF HPA PCB Connector Pin Assignments

2. Circuit Description

The HPA circuit is straight forward, routing signals from input SMA connectors to the amplifiers, the relay and to the output SMA connector. The preamplifiers are Avantec UTC-552 TO-8 can amplifiers. They use a +5 VDC power supply and are internally capacitively decoupled at the input and output and matched to a 50 Ohm impedance. The power supplied for the preamplifiers is filtered at the power input to the amplifiers using capacitors.

The final power amplifiers have 4 internal stages. They require a special external decoupling network for the power supply due to the high gain of the four stages. The decoupling network uses surface mount components to achieve a compact design and prevent conventional component leads from becoming transmission lines and coupling together. The decopuling network is similar to one recommended by the manufacturer [Ref.5].

Power control is accomplished using a 0 to +5 VDC control signal. This will vary output power from 0 dBm to +37 dBm. The power control signal is externally generated in the RF power and control section. Figure 11 shows a "T" surface mount resistor network. It is placed in the RF signal path immediately after its entry on the PCB through the SMA connectors. This network will allow fine tuning of the RF signal level during the testing of the PCB.

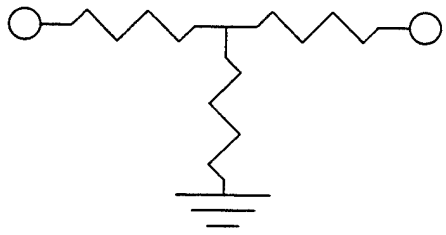


Figure 11 Resistive "T" Network

3. Power Requirements

The UTC-552 amplifier requires 18 mA at +5 VDC for a total power of 90 mW. The final power amplifier is 45% efficient. The final power amplifier requires 11.1 W to produce 5 W RF output power. The relay requires 20 mA at +5V when switched to the normally open position, for a power of 100 mW. The total power required for RF HPA PCB is 11.3 W.

4. Printed Circuit Board Layout

The RF HPA PCB, using micro strip circuit construction, is composed of 2 layers with an FR-4 dielectric between the layers. Appendix E describes micro strip circuit construction. Figure 12 shows a cross section of the RF HPA PCB. Surface mount components are used in the RF signal path. This required the use of a micro strip circuit.

The final power amplifiers, shown in Figure 13, require mounting to a heat sink. The amplifiers are mounted with their leads perpendicular to the PCB back to back on a block of aluminum. The aluminum block is also fastened to the PCB with screws, so it contacts the bottom ground plane of the PCB.

The micro strip width is calculated below, using Equation (6) and Equation (7) with $h = 31$ mil:

$$A = \frac{50}{60}\sqrt{\frac{4.6+1}{2}} + \frac{4.6-1}{4.6+1}\left(0.23 + \frac{0.11}{4.6}\right) = 1.5577$$

$$W = 31\frac{8e^{1.5577}}{e^{2(1.5577)} - 2} = 57\ mil$$

This is approximately double the width of a stripline trace of the same characteristic impedance.

The HPA printed circuit board as well as the other printed circuit boards are designed to meet the functional requirements of PANSAT. The materials and construction techniques used represent those currently used in industry. The following chapter provides an analysis of the PCB designs with recommendations and conclusions.

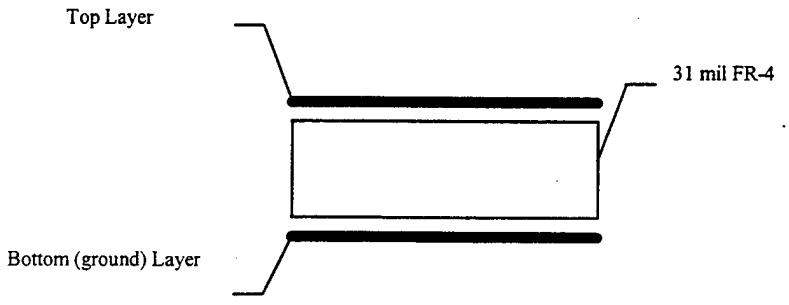
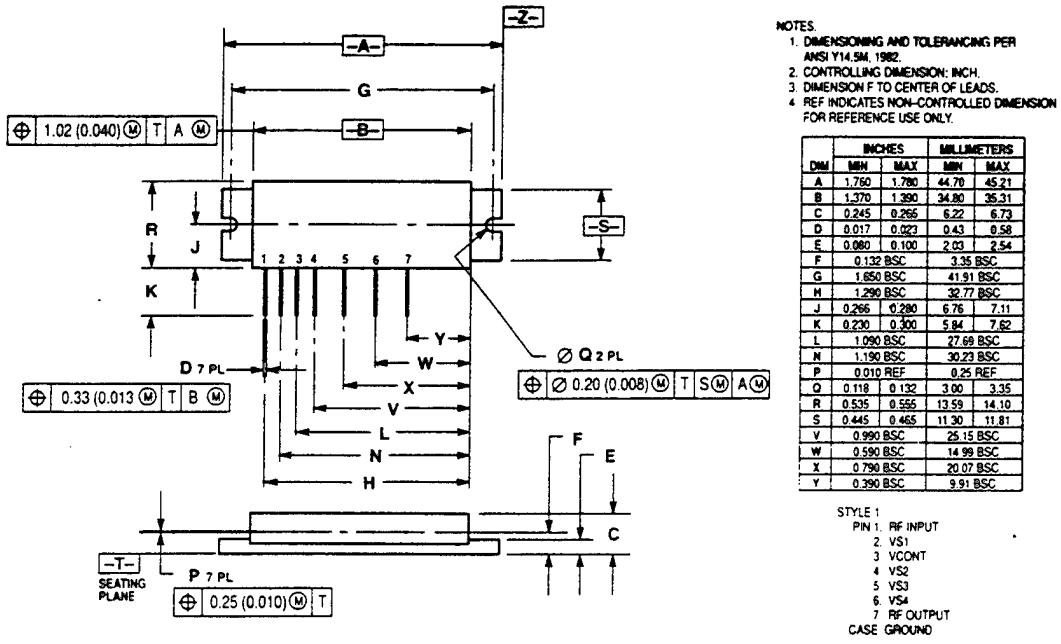


Figure 12 RF HPA PCB Cross Section



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.760	1.780	44.70	45.21
B	1.370	1.390	34.80	35.31
C	0.245	0.265	6.22	6.73
D	0.017	0.023	0.43	0.58
E	0.080	0.100	2.03	2.54
F	0.132 BSC		3.35 BSC	
G	1.650 BSC		41.91 BSC	
H	1.290 BSC		32.77 BSC	
J	0.266	0.280	6.76	7.11
K	0.230	0.300	5.84	7.62
L	1.090 BSC		27.69 BSC	
N	1.190 BSC		30.23 BSC	
P	0.010 REF		0.25 REF	
Q	0.118	0.132	3.00	3.35
R	0.535	0.555	13.59	14.10
S	0.445	0.465	11.30	11.81
V	0.990 BSC		25.15 BSC	
W	0.590 BSC		14.99 BSC	
X	0.790 BSC		20.07 BSC	
Y	0.390 BSC		9.91 BSC	

Figure 13 RF HPA Final Power Amplifiers. From Ref.[5].

IV. ANALYSIS AND CONCLUSIONS

A. ANALYSIS

1. Link Budget

The link budget PANSAT is computed in detail in Appendix F. Table 11 in Appendix F shows the link margin for the RF Subsystem PCB design. The link margin is positive for both up link and down link, indicating that the communications link will be closed in both directions.

The link budget would be improved by using a high gain directional antenna on the spacecraft. This is not possible because PANSAT is a free tumbling satellite with no attitude control. The link budget assumes that PANSAT is at 10 degrees above the horizon, in rain and at the highest data rate. This is a worst case scenario and transmit power may be reduced if any conditions improve.

2. Power Budget

The receive mode requires the LNA PCB and the Switching PCB for operation. The HPA PCB will remain without power to prevent any attempt to transmit during a receive operation. This would cause an overdrive of the LNA amplifiers and cause their first stages to be destroyed, rendering them useless. A hard logic interlock in the RF control circuit will prevent the HPA section from receiving power at the same time the LNA section is receiving power. The total power required in the receive mode is 1.42 W.

During transmit operations power will be removed from the low noise amplifiers for the reason discussed above. The HPA PCB will have power applied, with only one

amplifier string in operation at a time. The switching PCB will also require power. The total power requirement is 12.1 W, for a 5 W RF output. This power requirement may be reduced by transmitting at a lower power.

B. CONCLUSIONS

The RF switching PCB has been manufactured and is in currently in testing. The LN PCB and HPA PCB are awaiting contract approval for manufacture. The use of state of the art computer aided design tools is critical to achieve a working product.

The time required to learn to use Cadence Design System's tools is much longer than initially anticipated. The tools are very powerful, but assume the user has a background in PCB design. Appendix D describes the basic steps of PCB design and provides a list of commonly used terms encountered in PCB design.

Printed circuit board design in the RF frequencies is almost a "black art." There is little written on practical steps for design and layout. The currently available texts provide the electromagnetic theory and some general construction techniques. Much of the design detail must be gained from practical experience in PCB design. A good contact for students pursuing work in this area in the future is needed.

APPENDIX A. RF SWITCHING PCB DETAILED DRAWINGS

This appendix contains the detailed schematic, photoplot and assembly drawings for the RF switching PCB. The photoplot, assembly and physical dimension drawings are reduced to 64% of their original size for inclusion in this appendix. The following drawings are included:

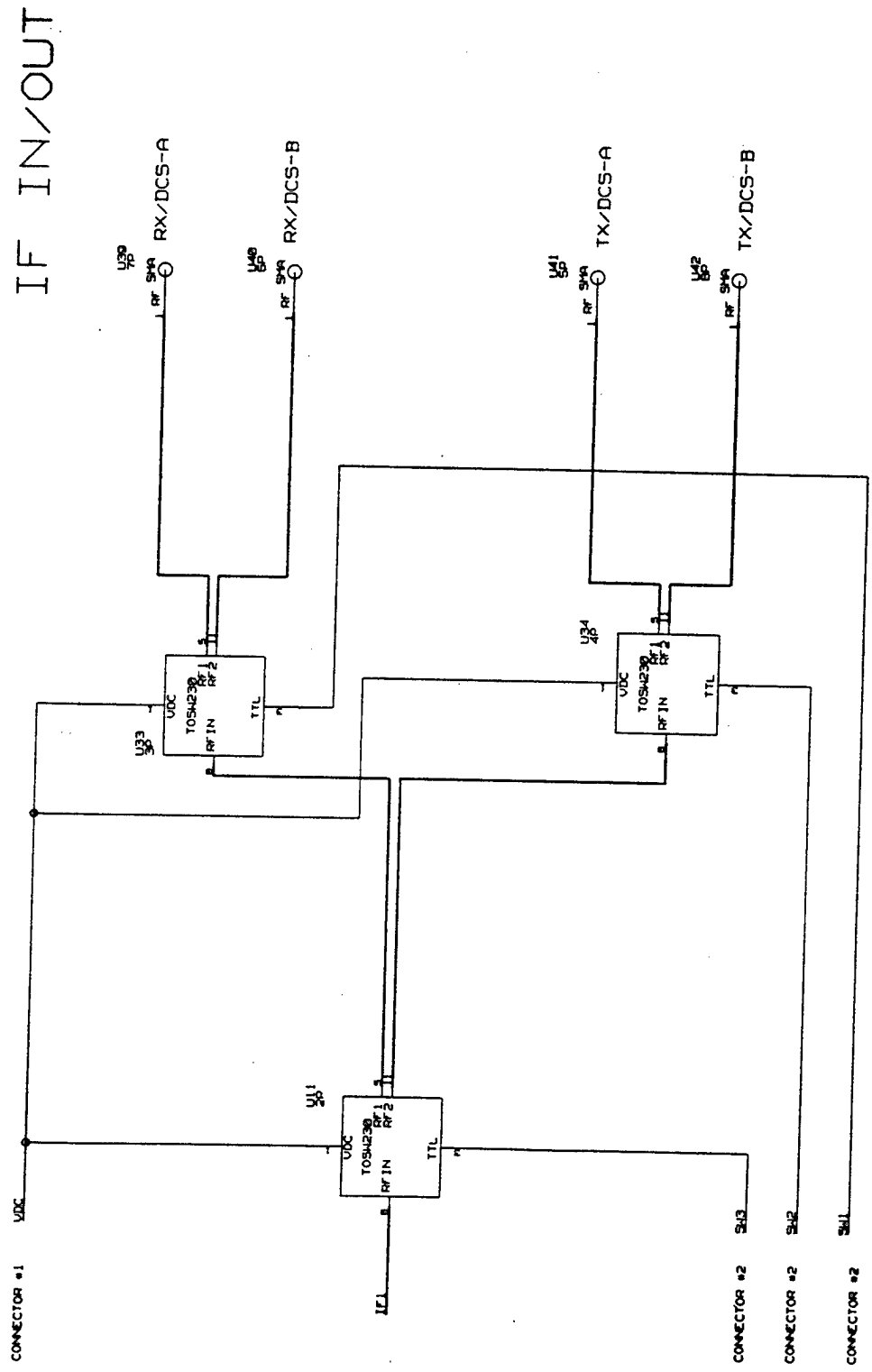


Figure 14 RF Switching Circuit Schematic - IF Section

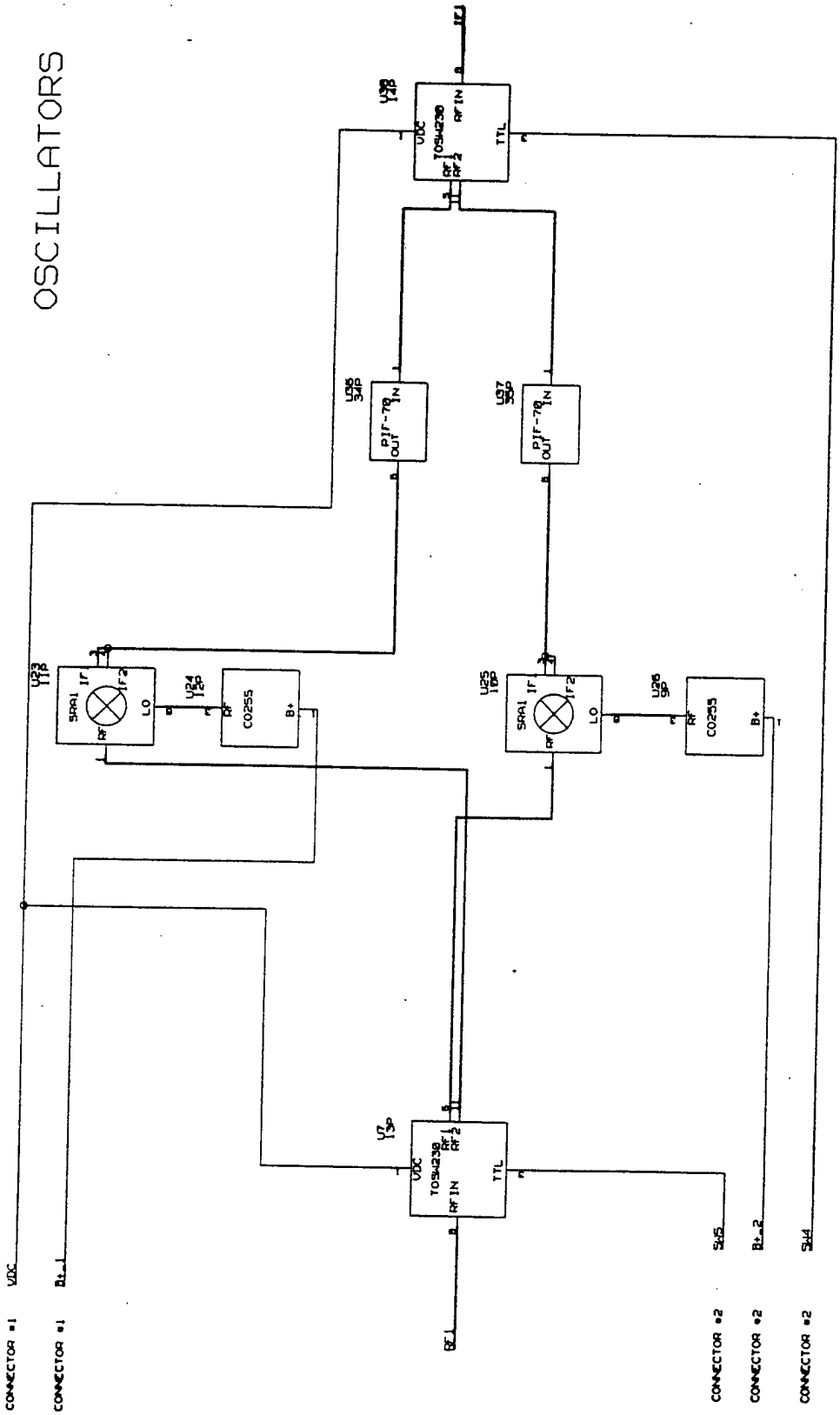


Figure 15 RF Switching Circuit Schematic- Oscillator Section

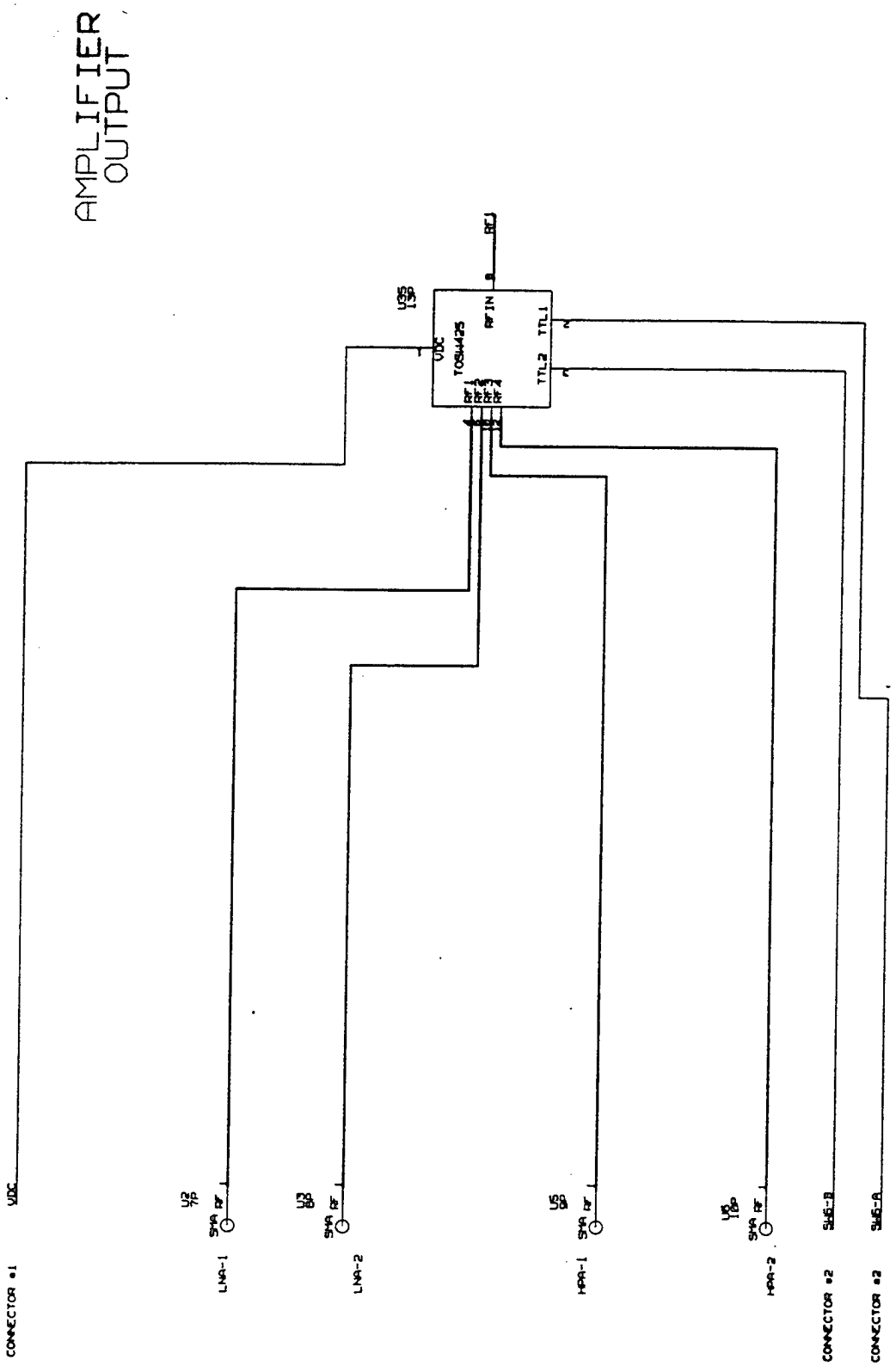


Figure 16 RF Switching Circuit Schematic - Amplifier Section

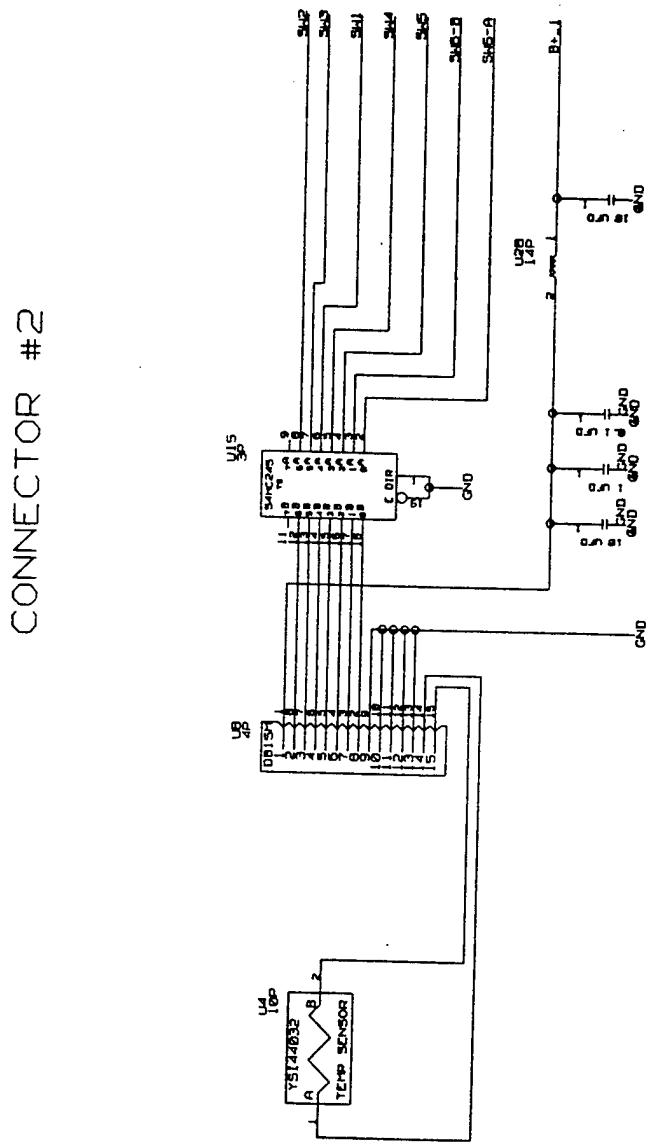


Figure 17 RF Switching Circuit Schematic - Connector #2

CONNECTOR #1

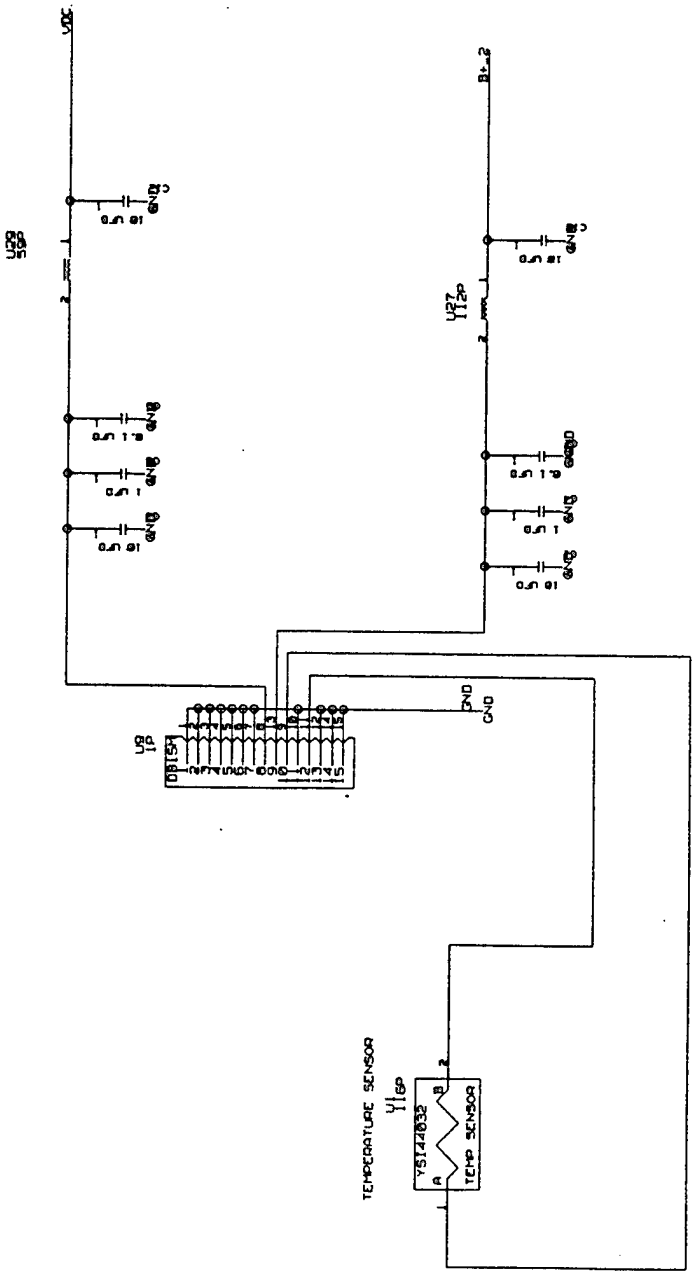


Figure 18 RF Switching Circuit Schematic - Connector #1

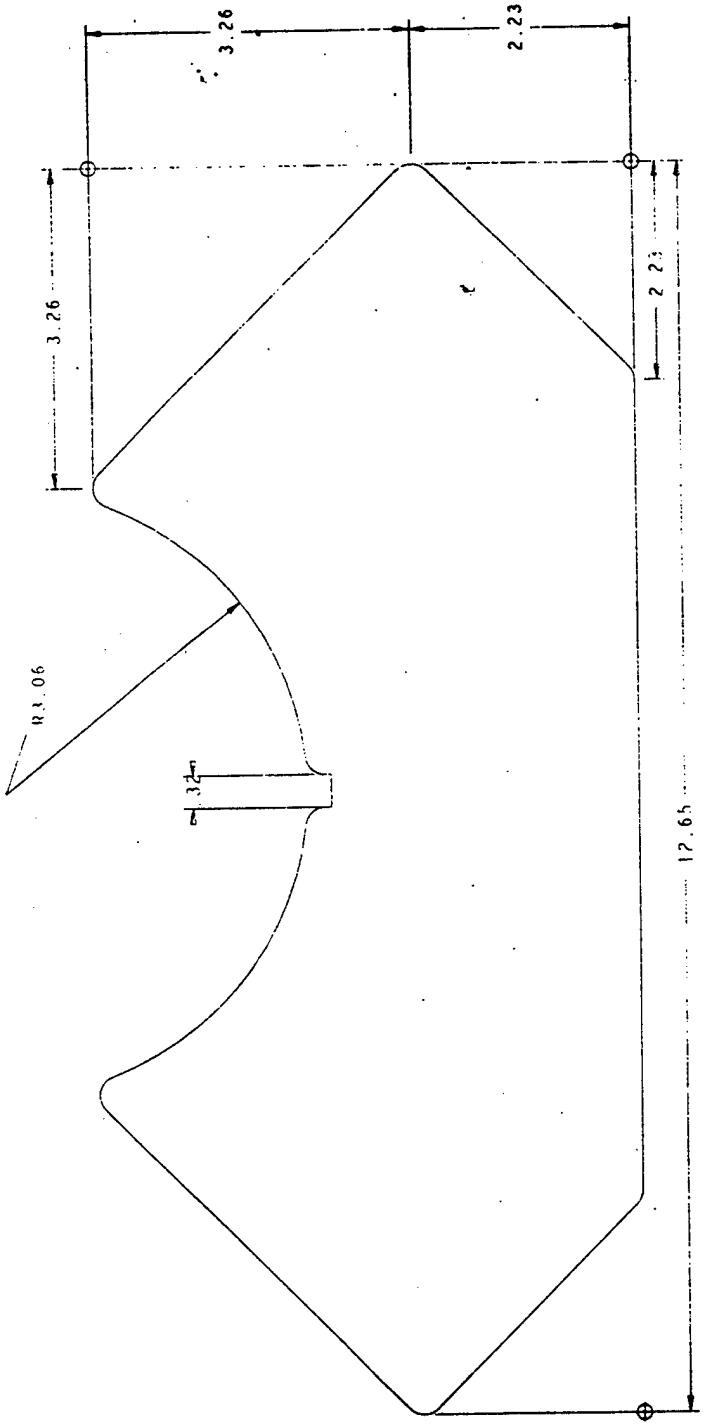


Figure 19 RF Switching PCB - Physical Size

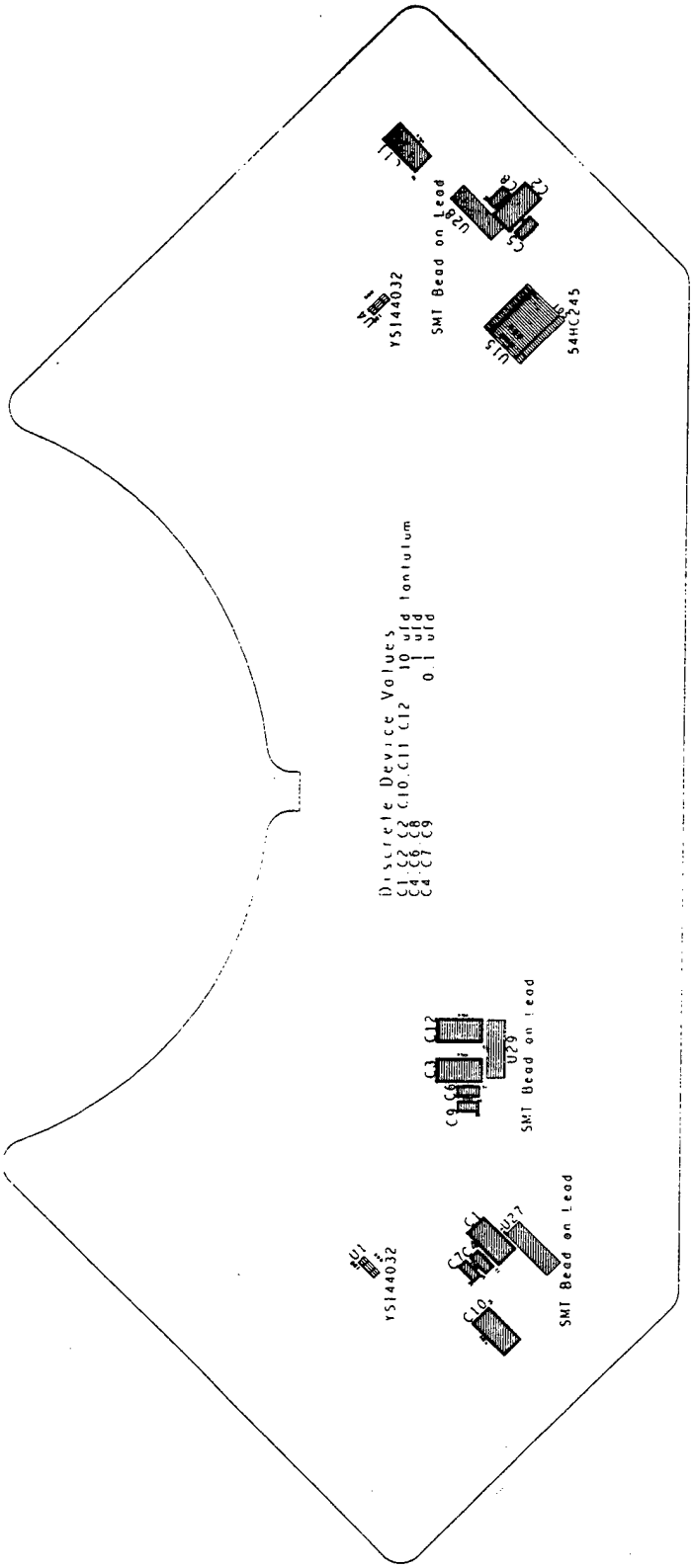


Figure 20 RF Switching PCB - Top Assembly Drawing

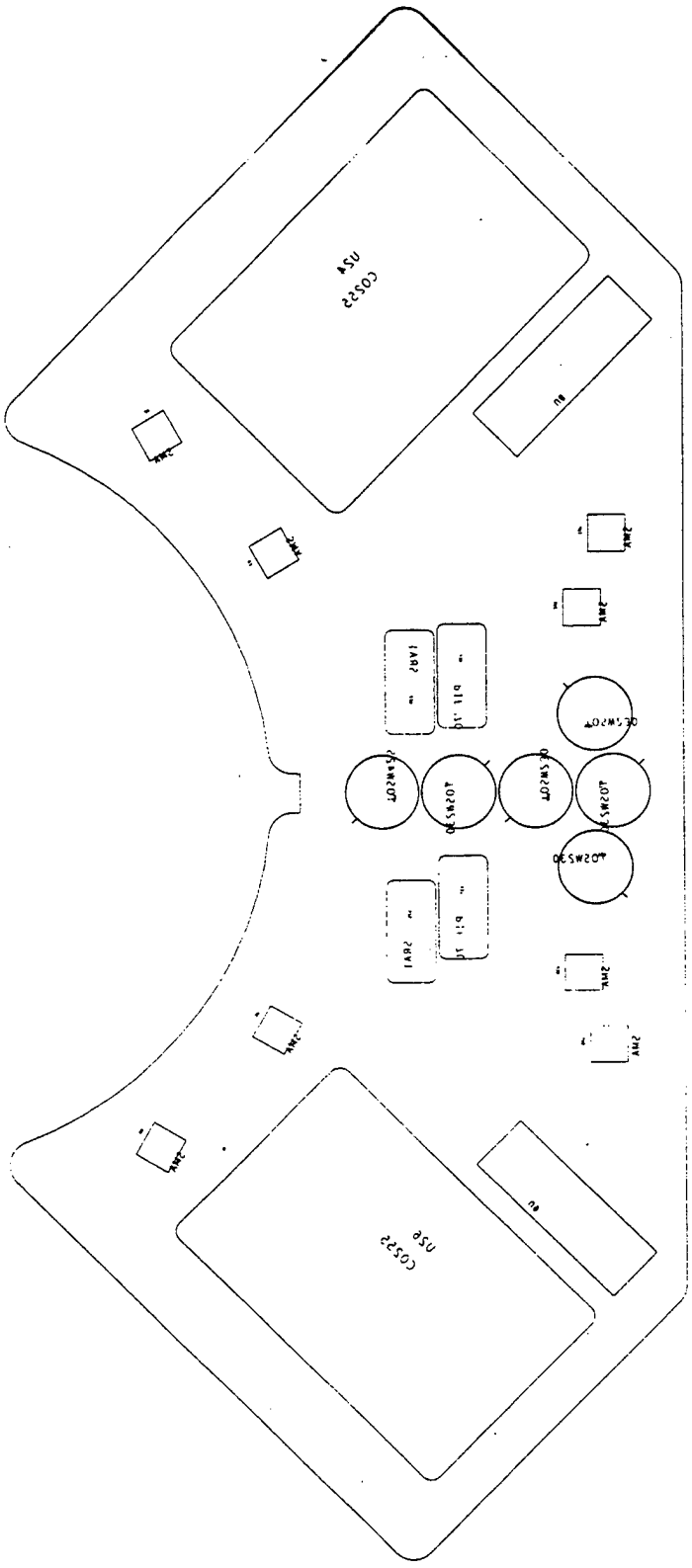


Figure 21 RF Switching PCB - Bottom Assembly Drawing

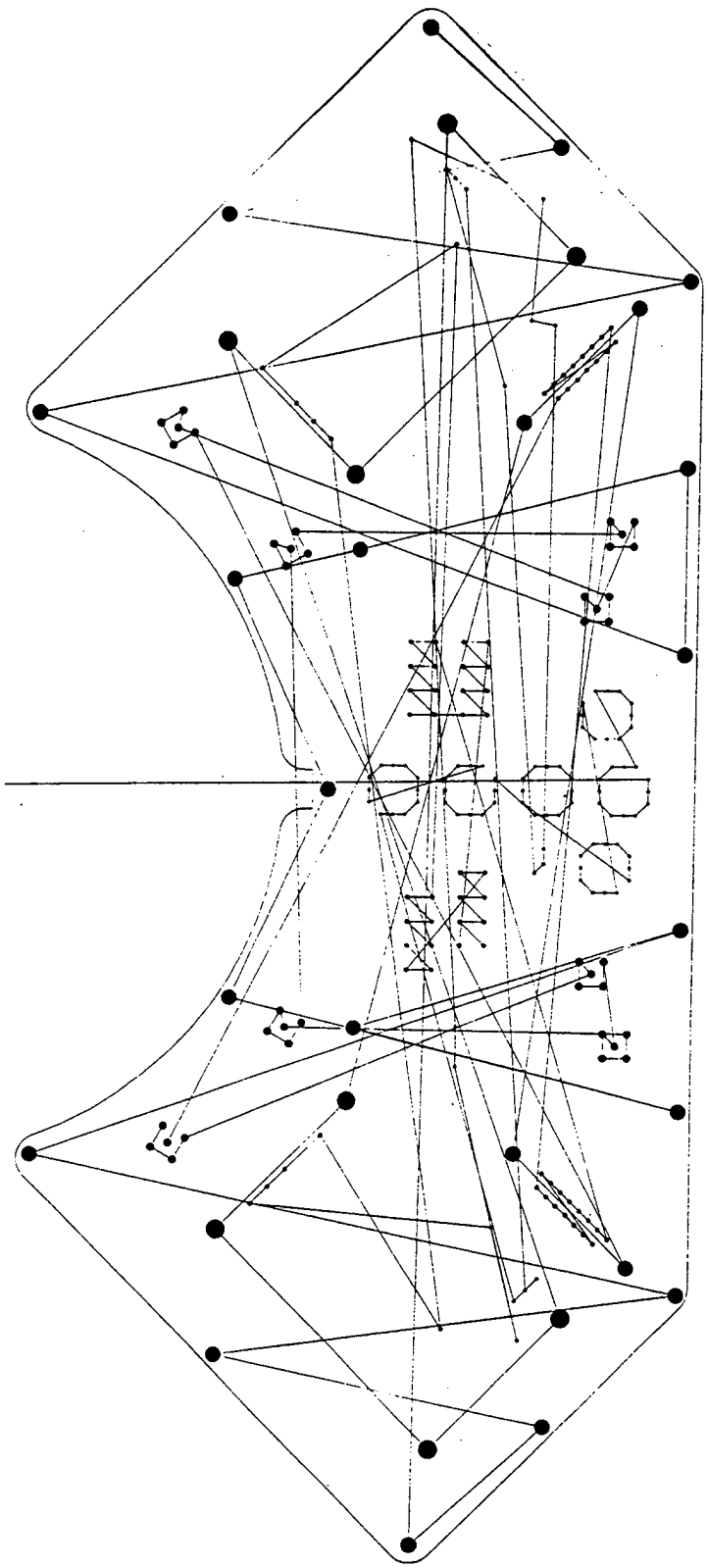


Figure 22 RF Switching PCB - NC Drill Drawing

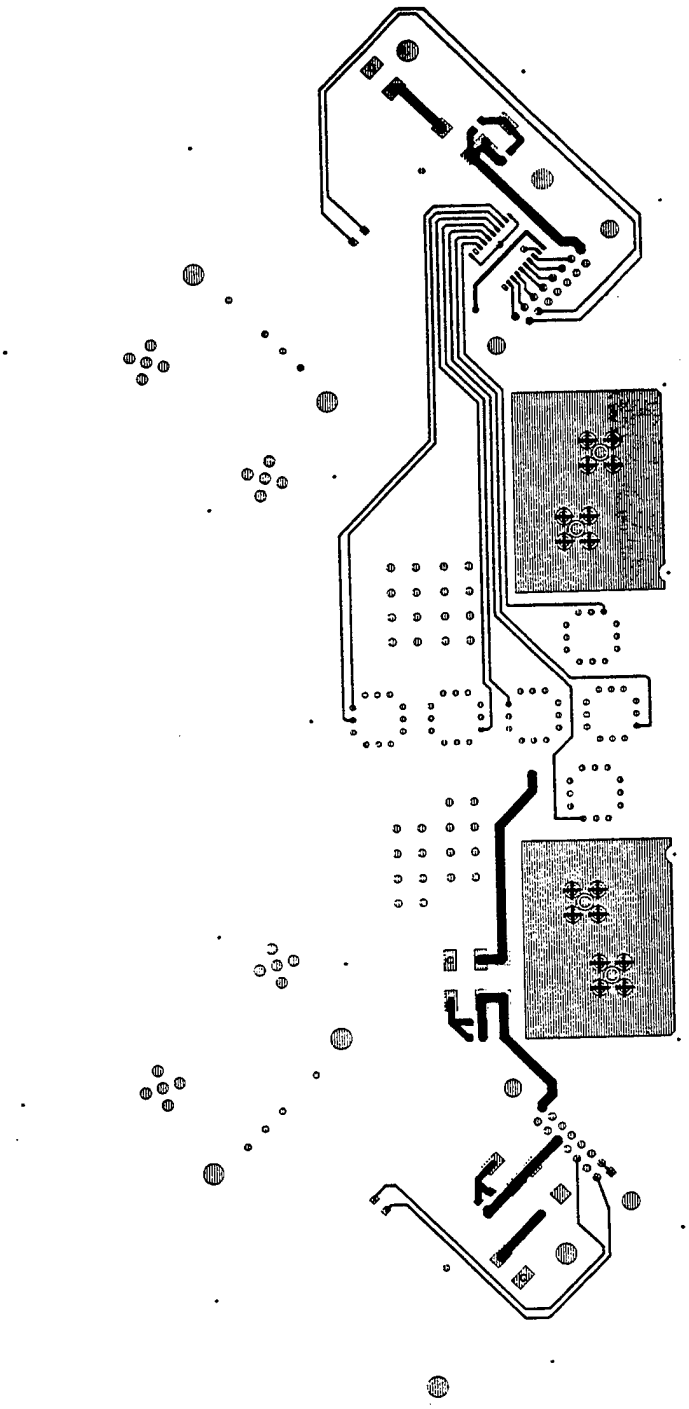


Figure 23 RF Switching PCB - Top Layer Photoplot

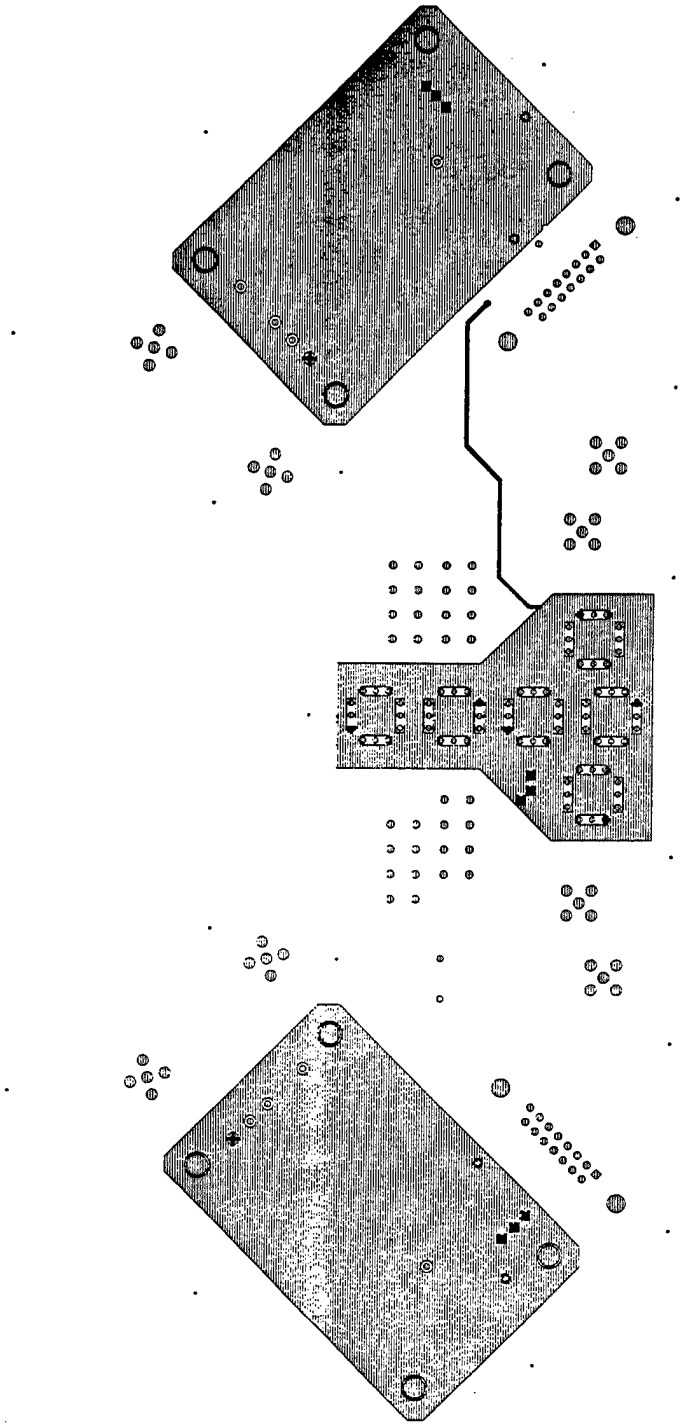


Figure 24 RF Switching PCB - Power Layer Photoplot

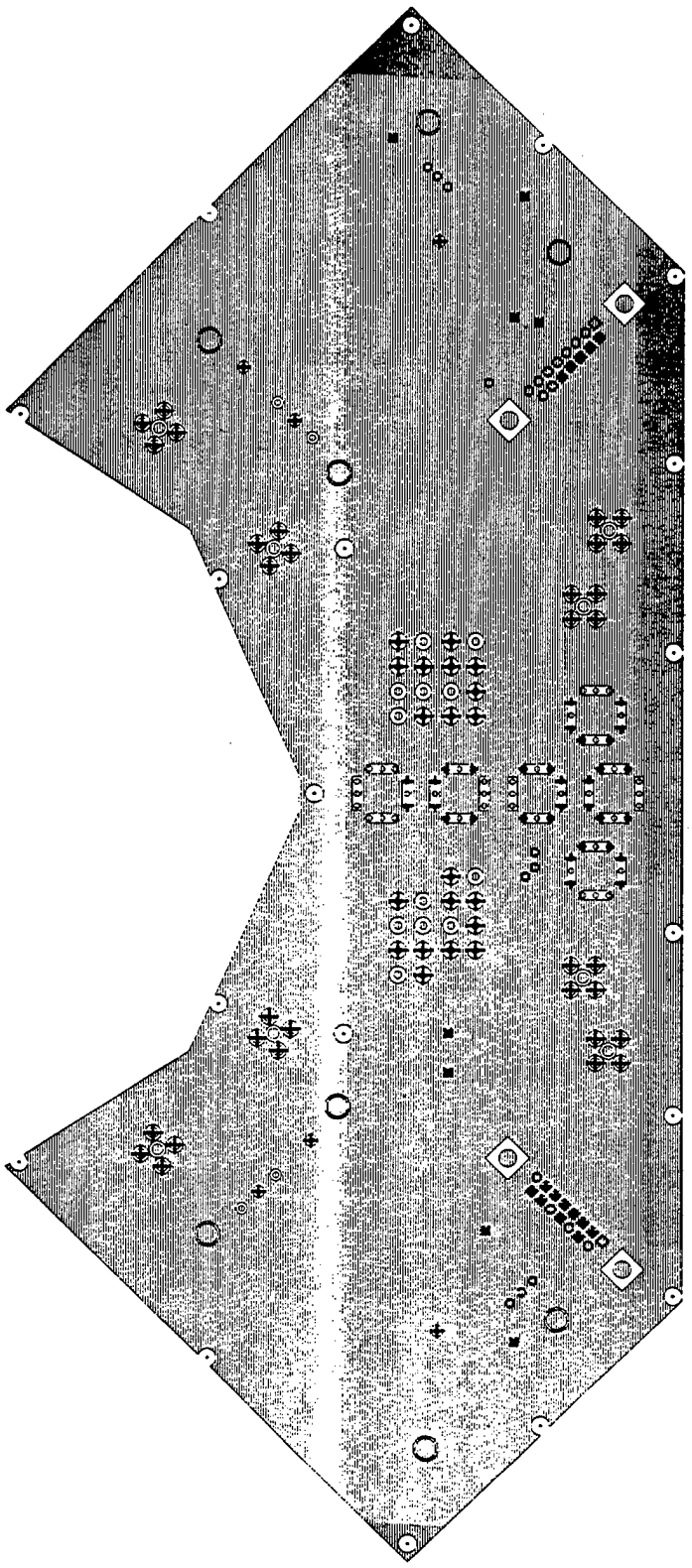


Figure 25 RF Switching PCB - Ground1 Layer Photoplot

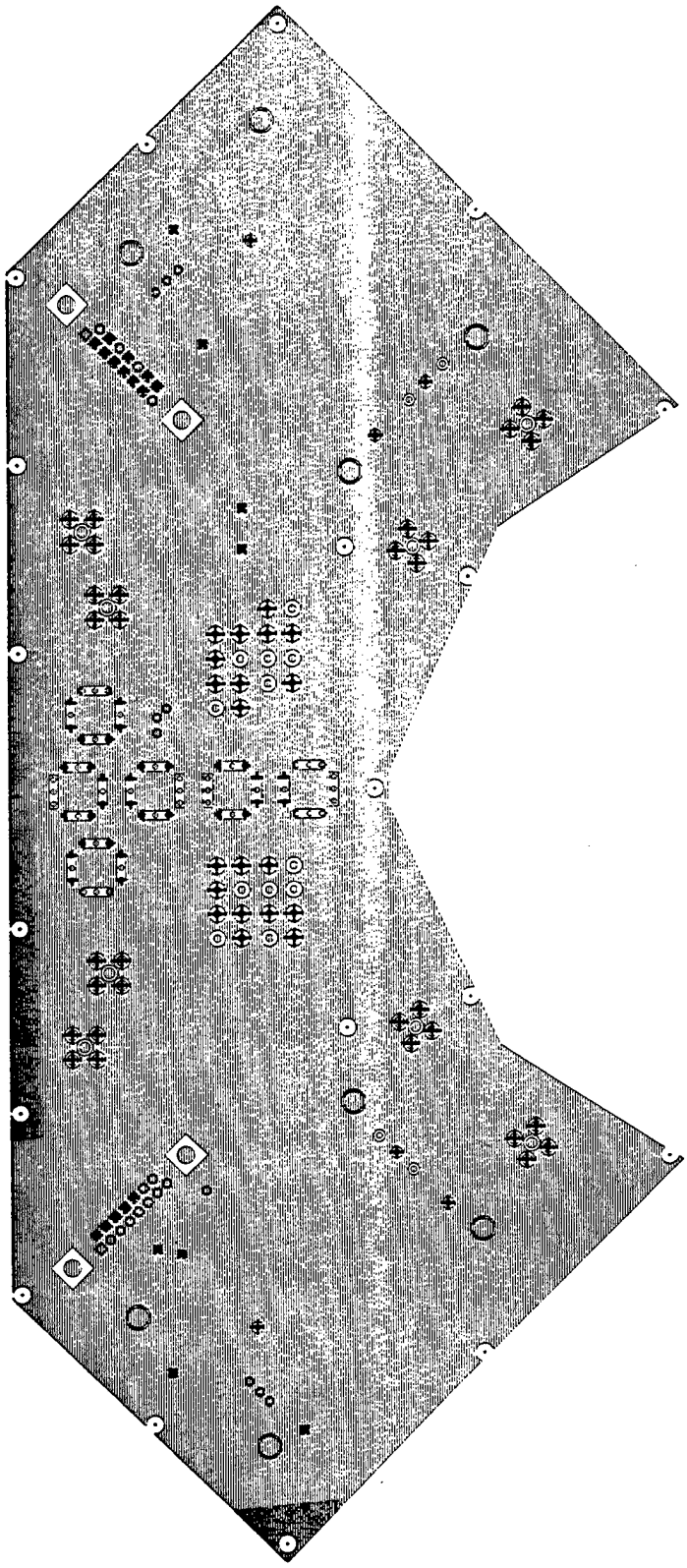


Figure 26 RF Switching PCB - Ground2 Layer Photoplot

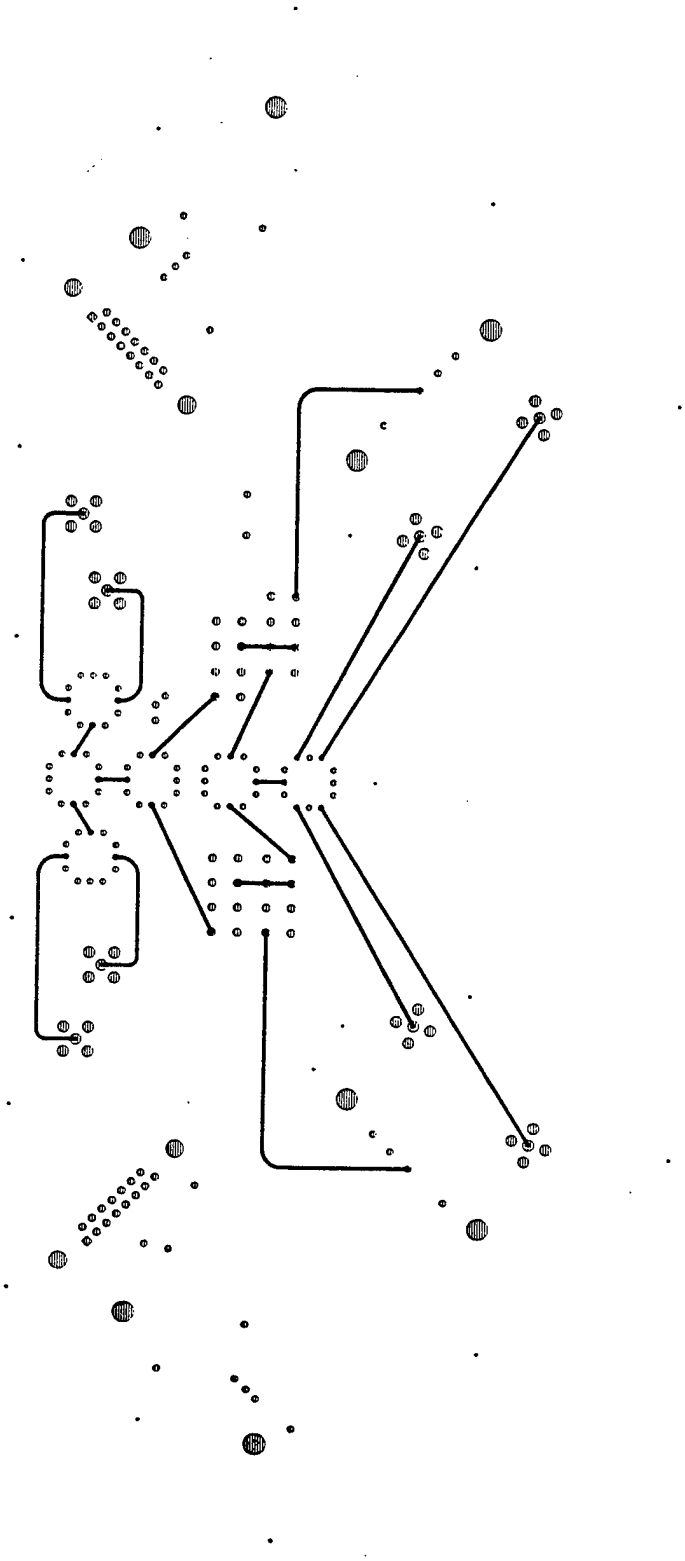


Figure 27 RF Switching PCB - RF signal Layer Photoplot

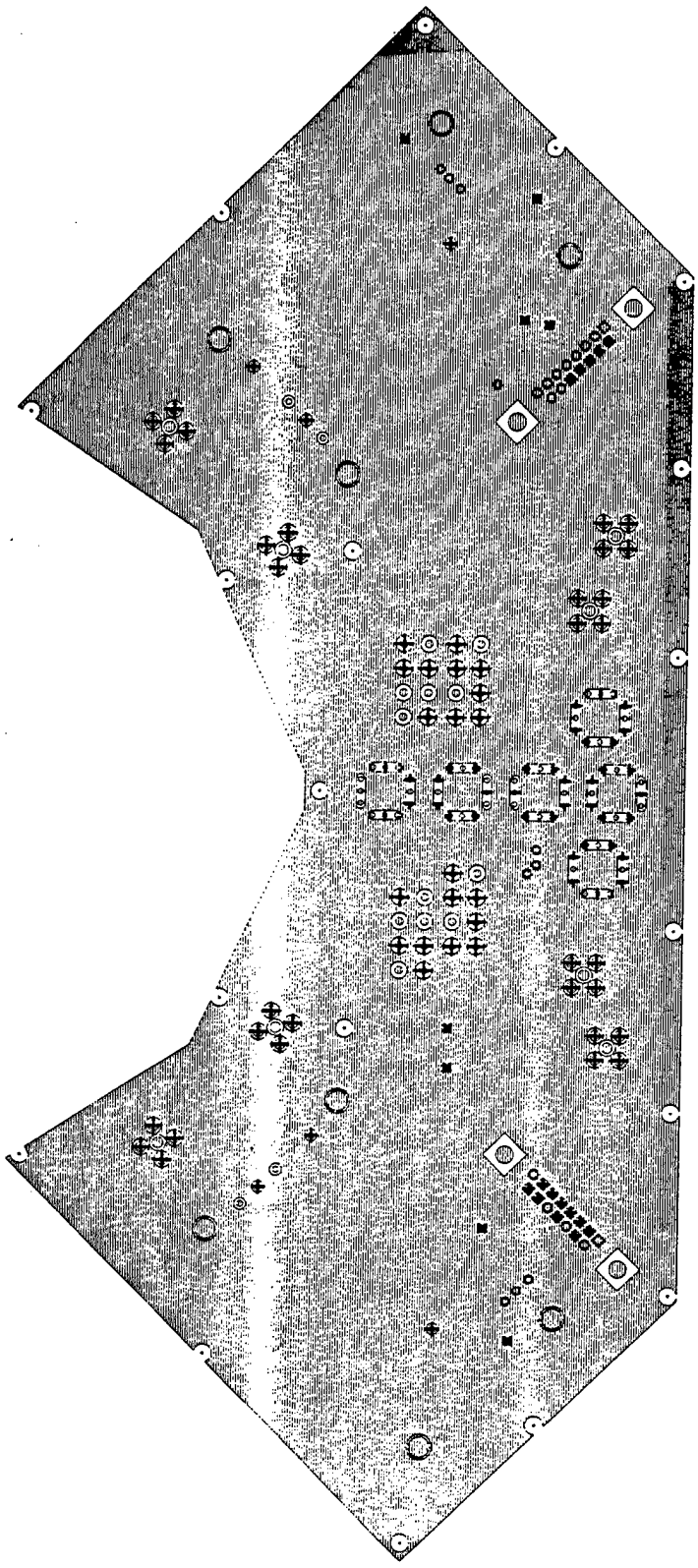


Figure 28 RF Switching PCB - Bottom (ground) Layer Photoplot

APPENDIX B. RF LNA PCB DETAILED DRAWINGS

This appendix contains the detailed schematic, photoplot and assembly drawings for the RF LNA PCB. The photoplot, assembly and physical dimension drawings are reduced to 64% of their original size for inclusion in this appendix. The following drawings are included:

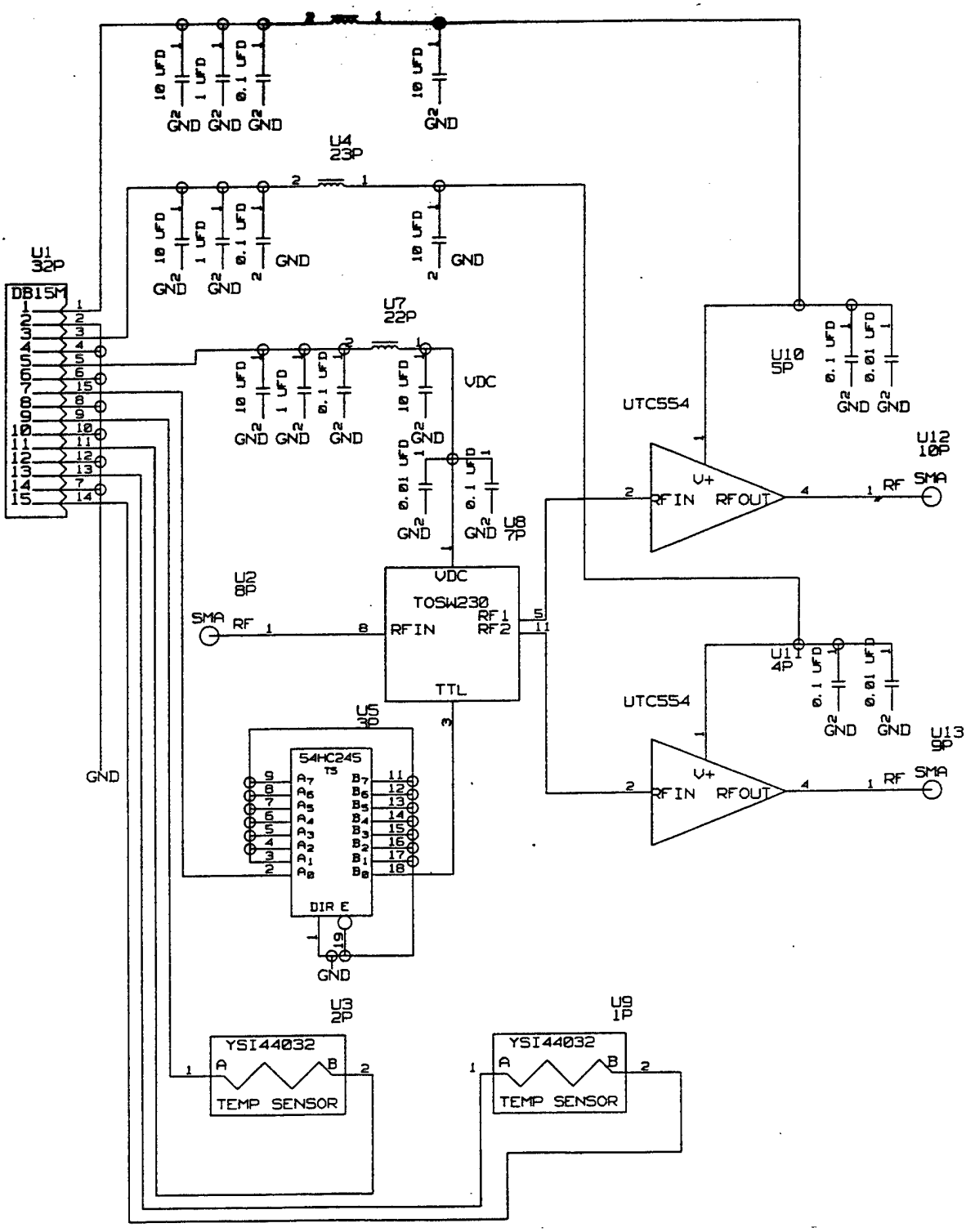


Figure 29 RF LNA Circuit Schematic

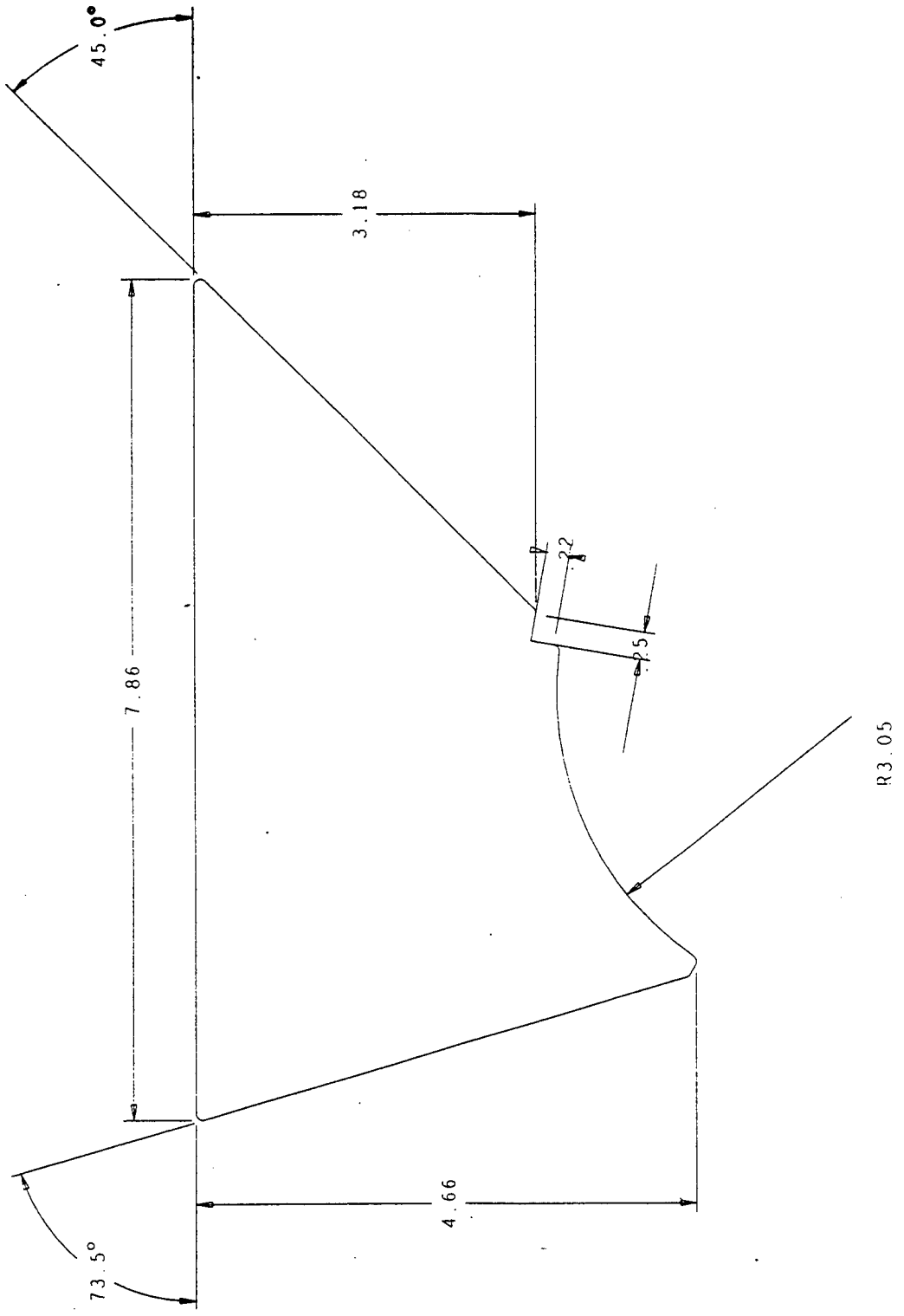


Figure 30 RF LNA PCB - Physical Size

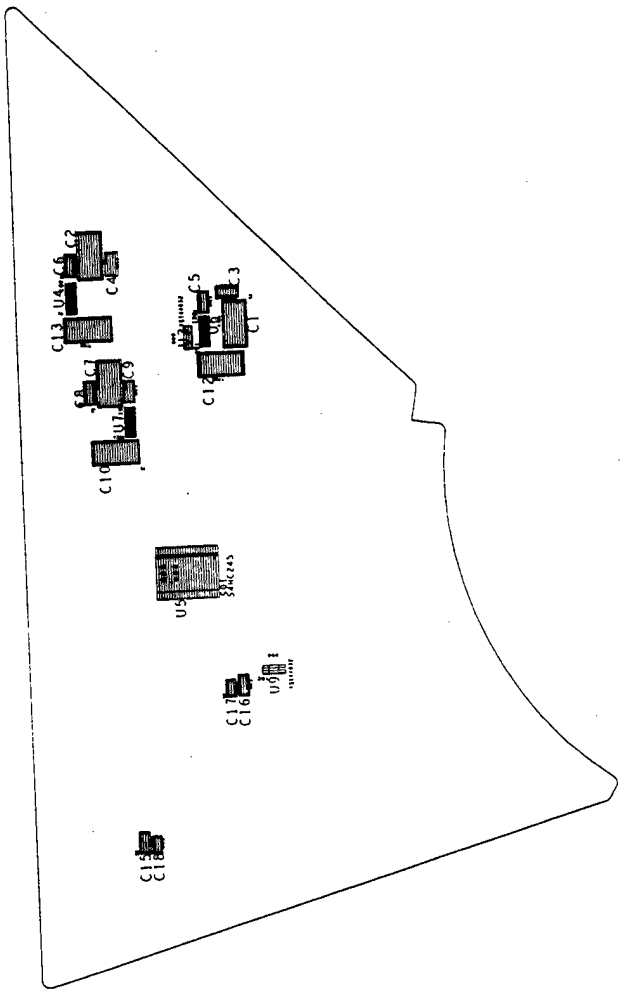


Figure 31 RF LNA PCB - Top Assembly Drawing

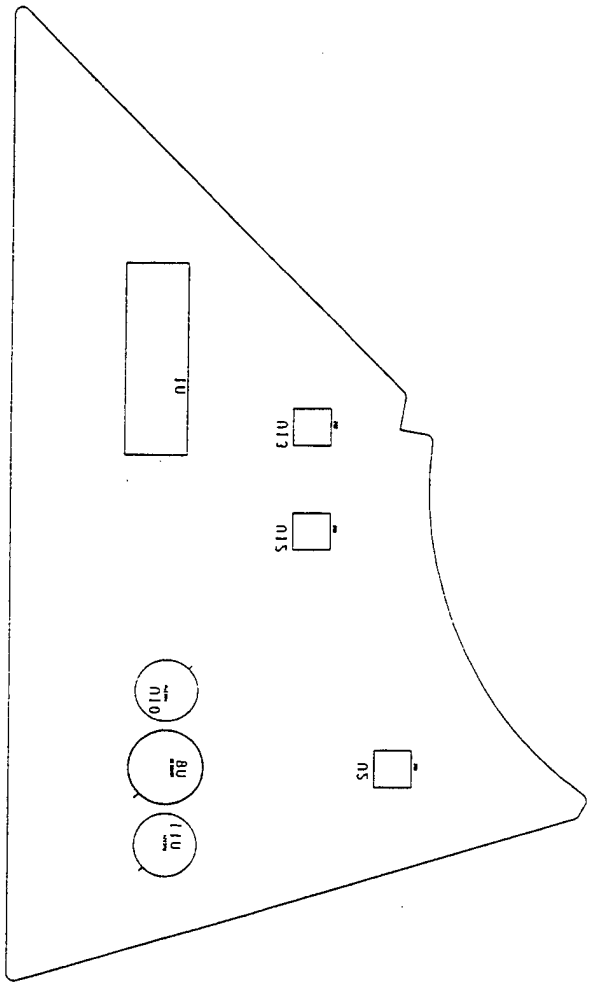


Figure 32 RF LNA PCB - Bottom Assembly Drawing

Figure 33 RF LNA PCB - NC Drill Drawing

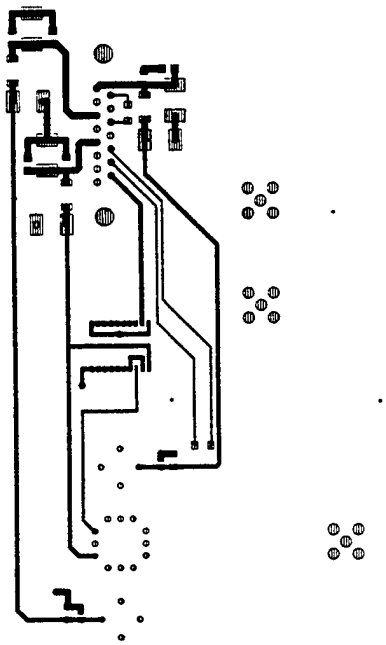


Figure 34 RF LNA PCB - Top Layer Photoplot

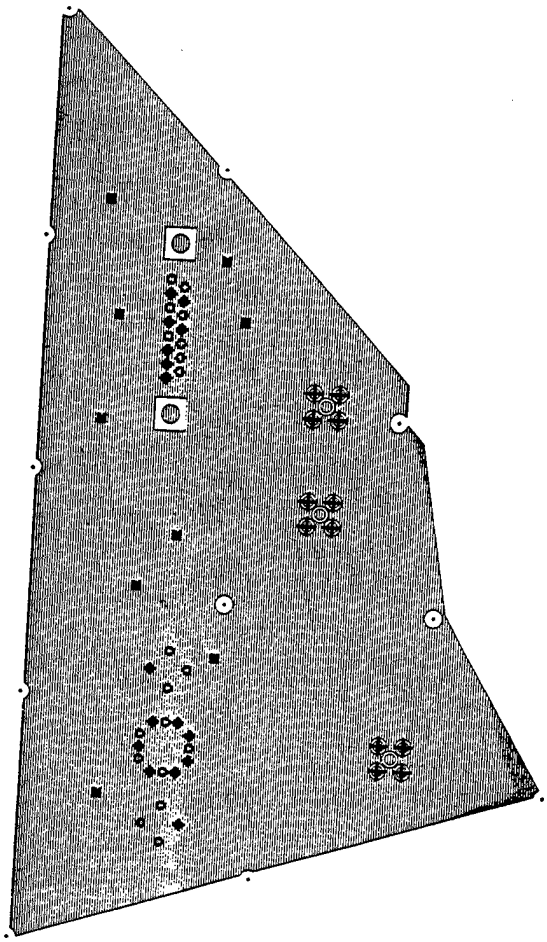


Figure 35 RF LNA PCB - Ground1 Layer Photoplot

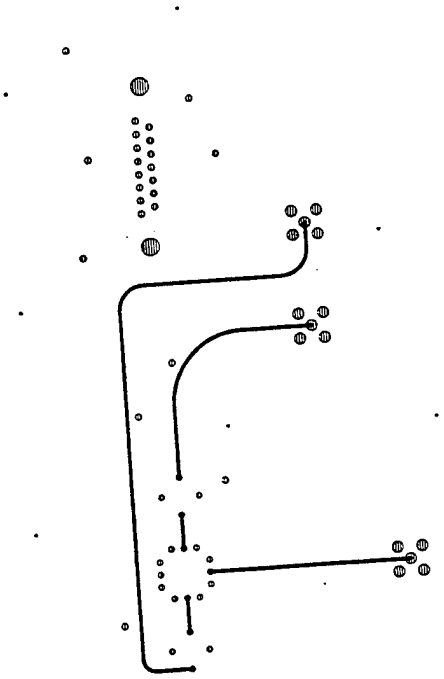


Figure 36 RF LNA PCB - RF signal Layer Photoplot

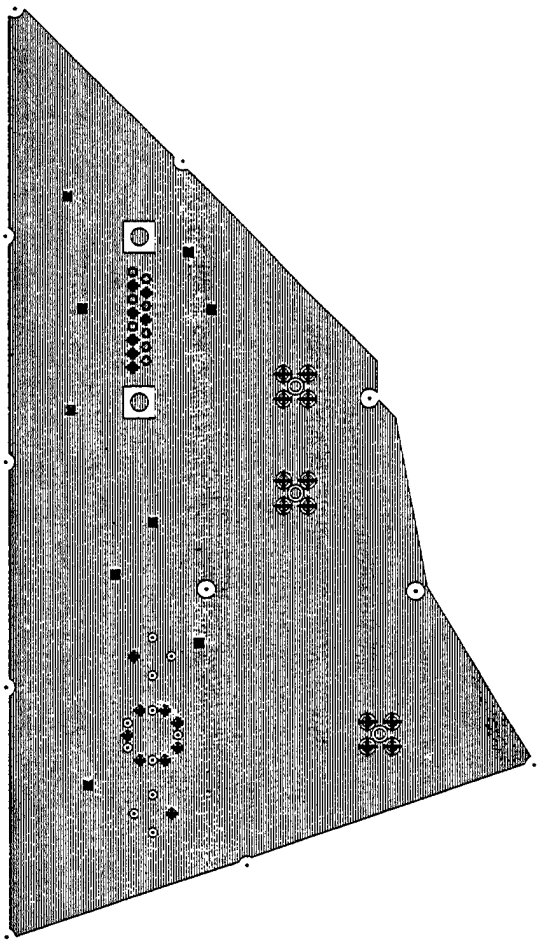


Figure 37 RF LNA PCB - Bottom (ground) Layer Photoplot

APPENDIX C. RF HPA PCB DETALED DRAWINGS

This appendix contains the detailed schematic, photoplot and assembly drawings for the RF HPA PCB. The photoplot, assembly and physical dimension drawings are reduced to 64% of their original size for inclusion in this appendix. The following drawings are included:

Figure 38 RF HPA Circuit Schematic- Input Section

Figure 39 RF HPA Circuit Schematic- Output Section

Figure 40 RF HPA PCB - Physical Size

Figure 41 RF HPA PCB - Top Assembly Drawing

Figure 42 RF HPA PCB - Bottom Assembly Drawing

Figure 43 RF HPA PCB - NC Drill Drawing

Figure 44 RF HPA PCB - Top Layer Photoplot

Figure 45 RF HPA PCB - Bottom (ground) Layer Photoplot

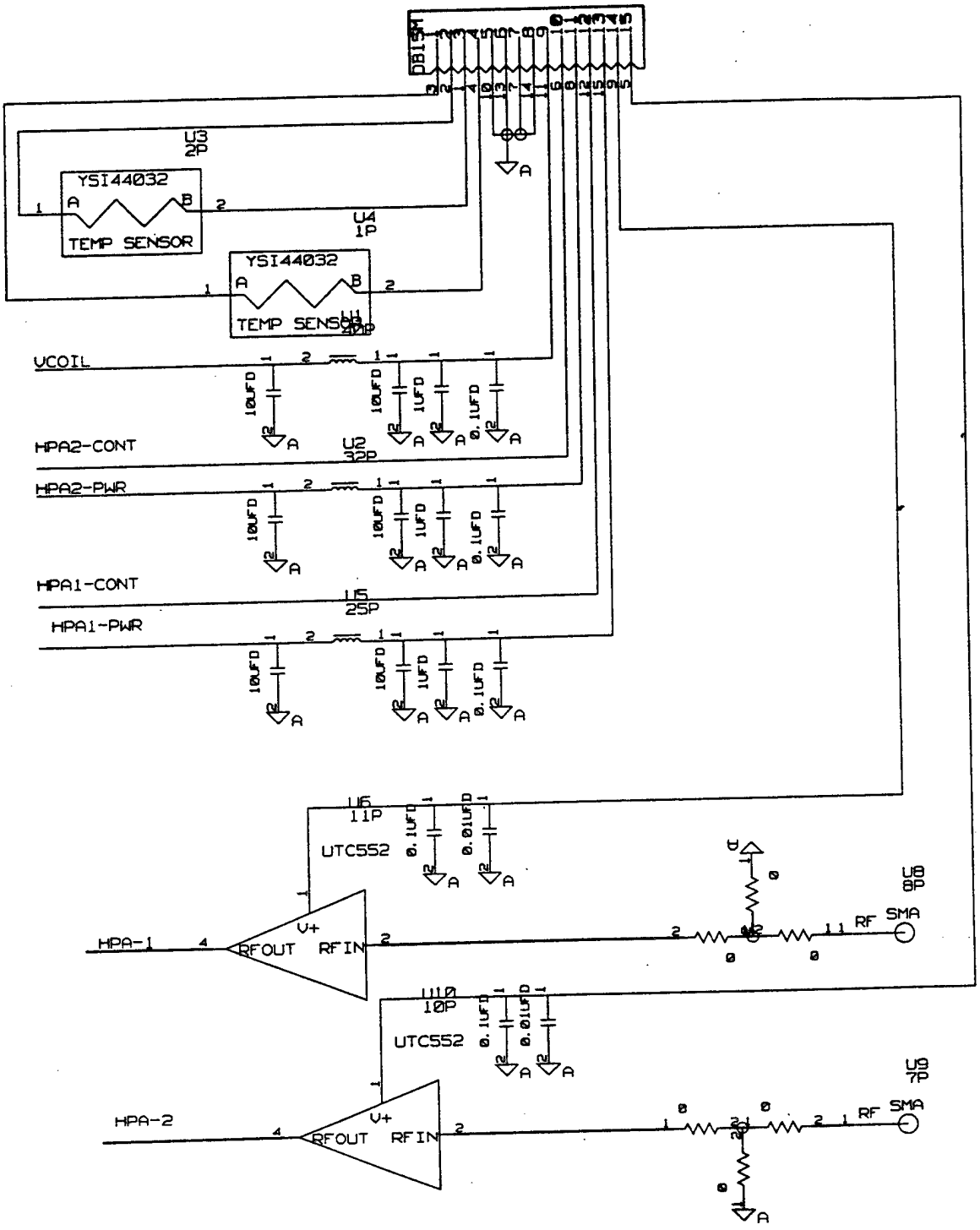


Figure 38 RF HPA Circuit Schematic- Input Section

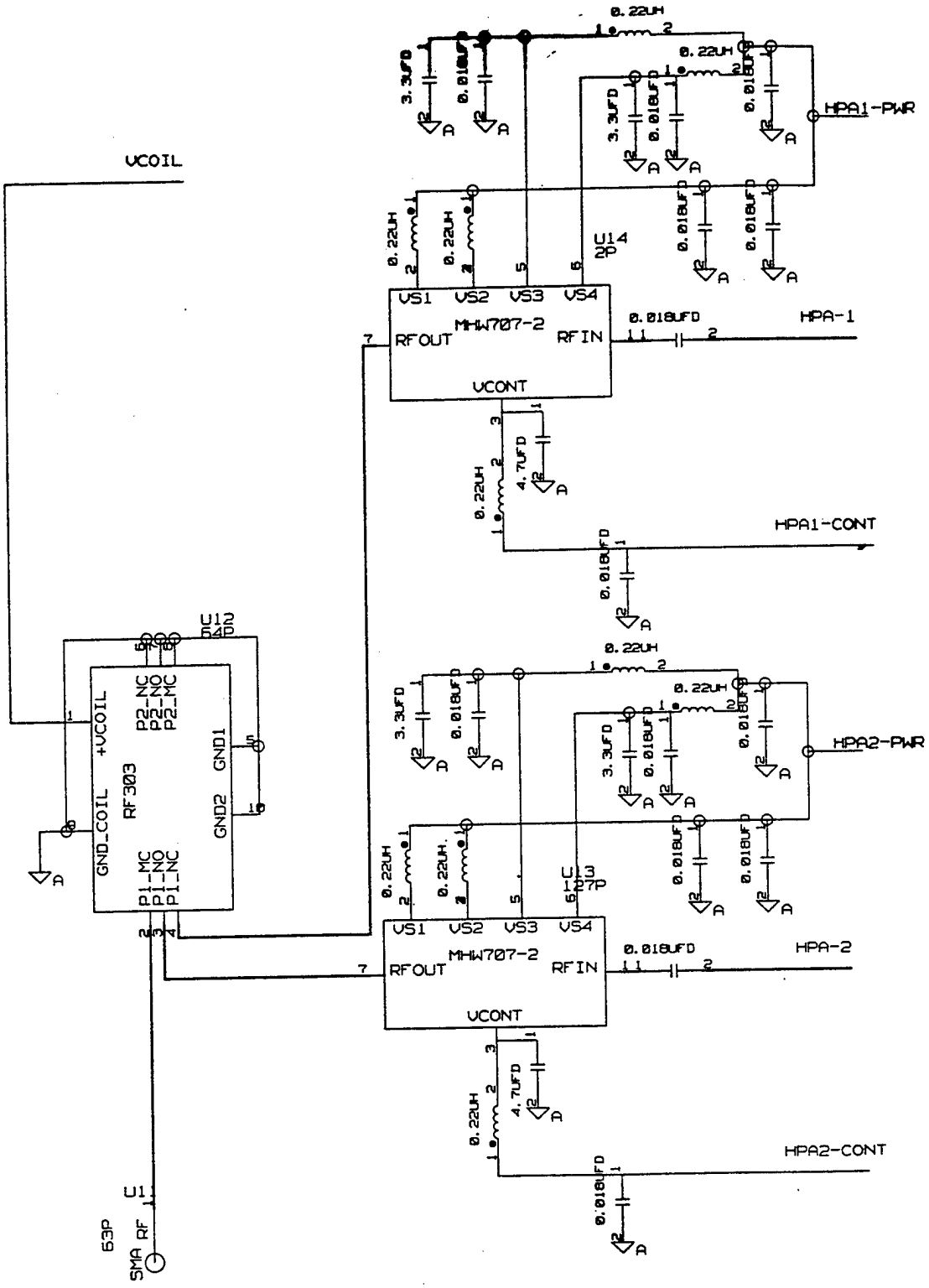


Figure 39 RF HPA Circuit Schematic- Output Section

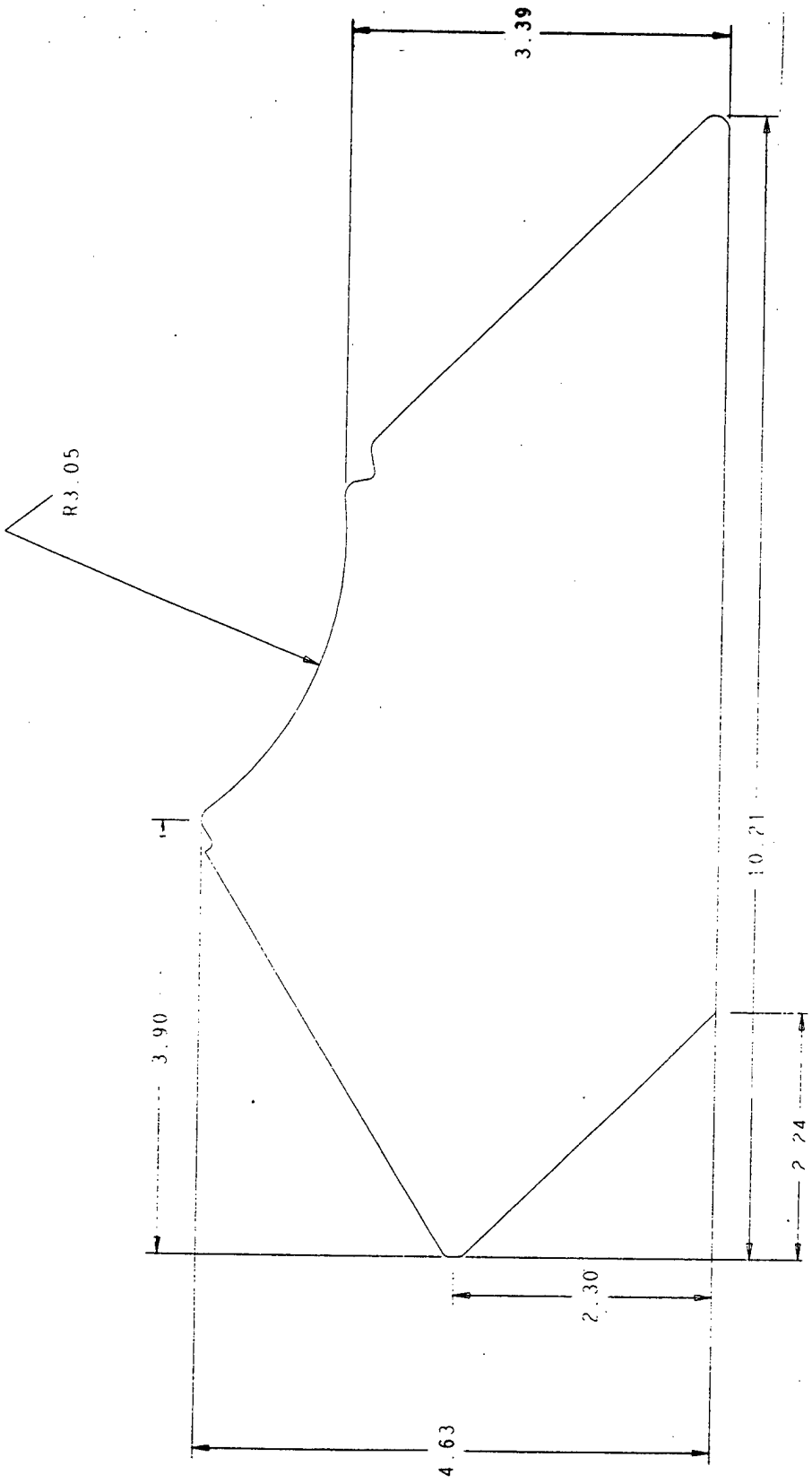


Figure 40 RF HPA PCB - Physical Size

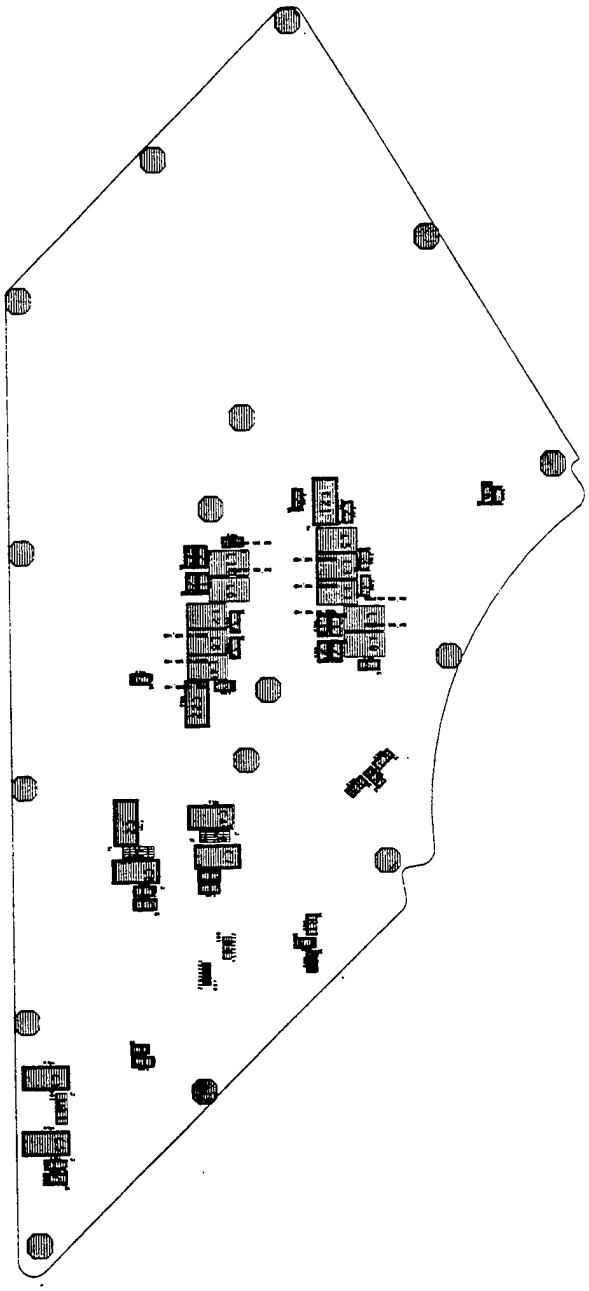


Figure 41 RF HPA PCB - Top Assembly Drawing

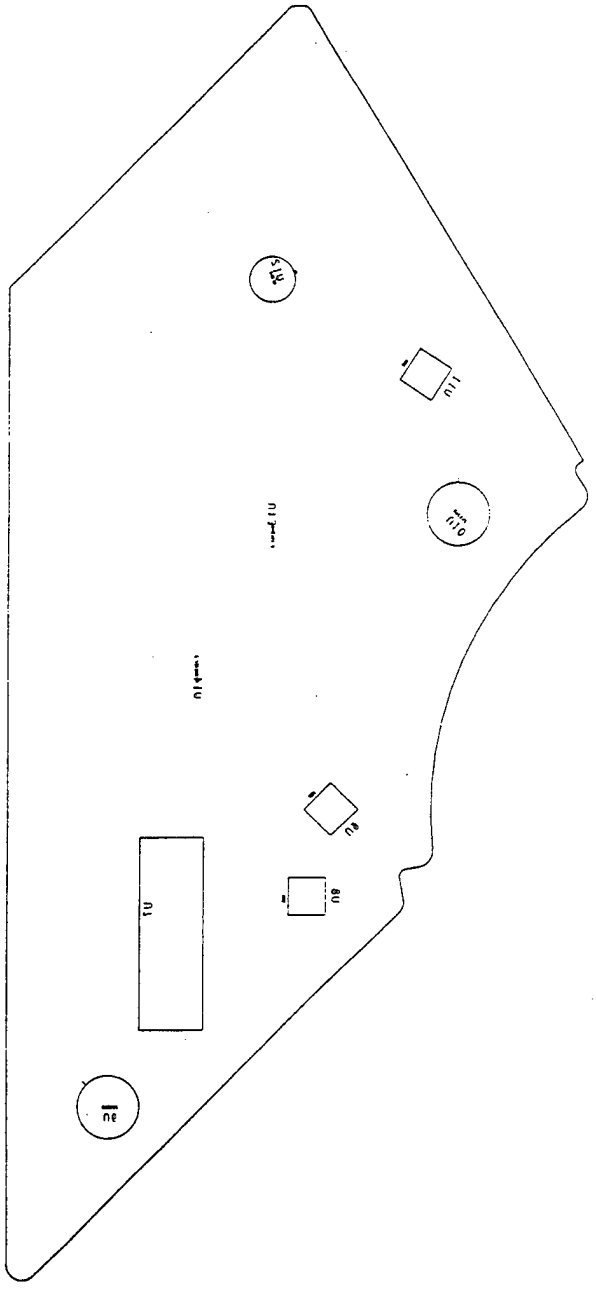


Figure 42 RF HPA PCB - Bottom Assembly Drawing

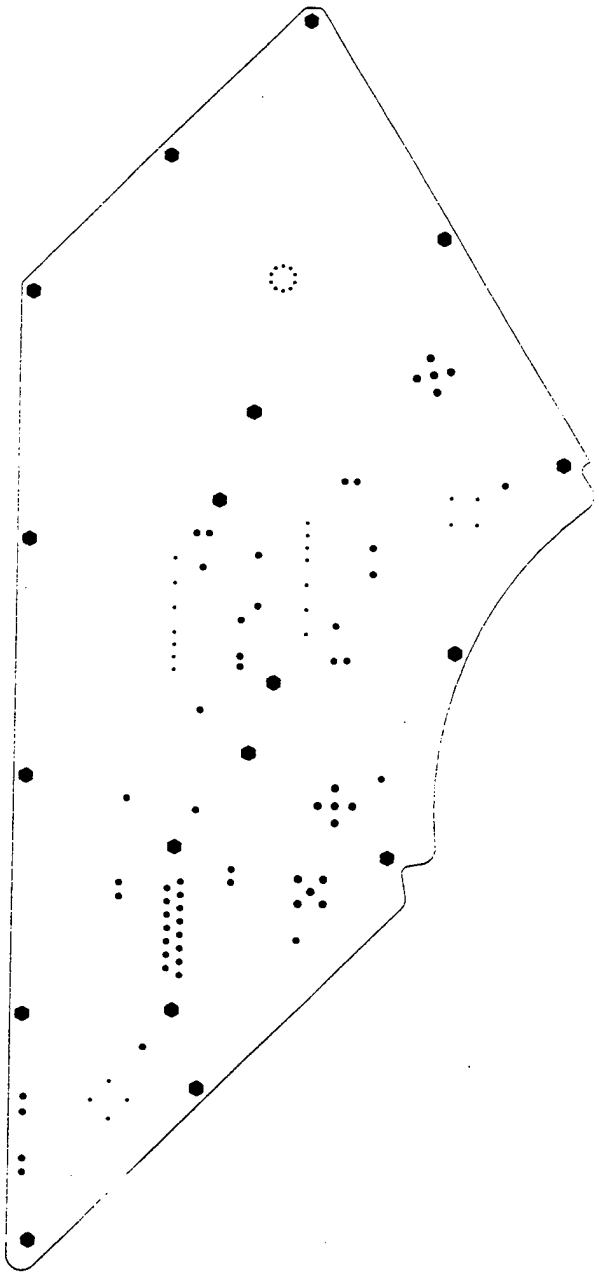


Figure 43 RF HPA PCB - NC Drill Drawing

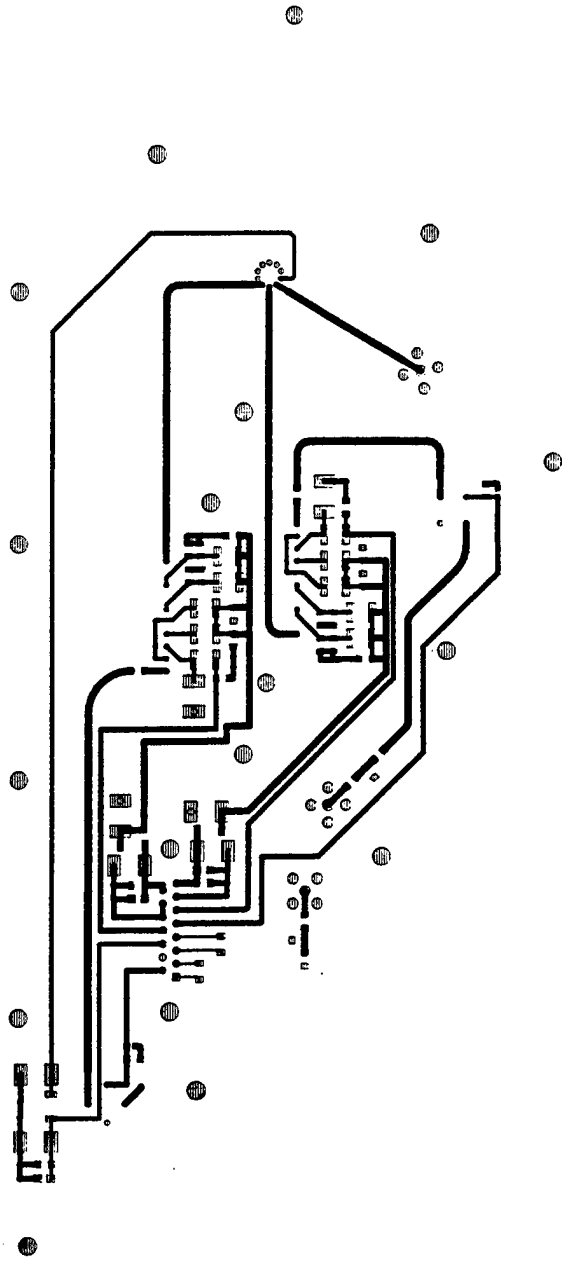


Figure 44 RF HPA PCB - Top Layer Photoplot

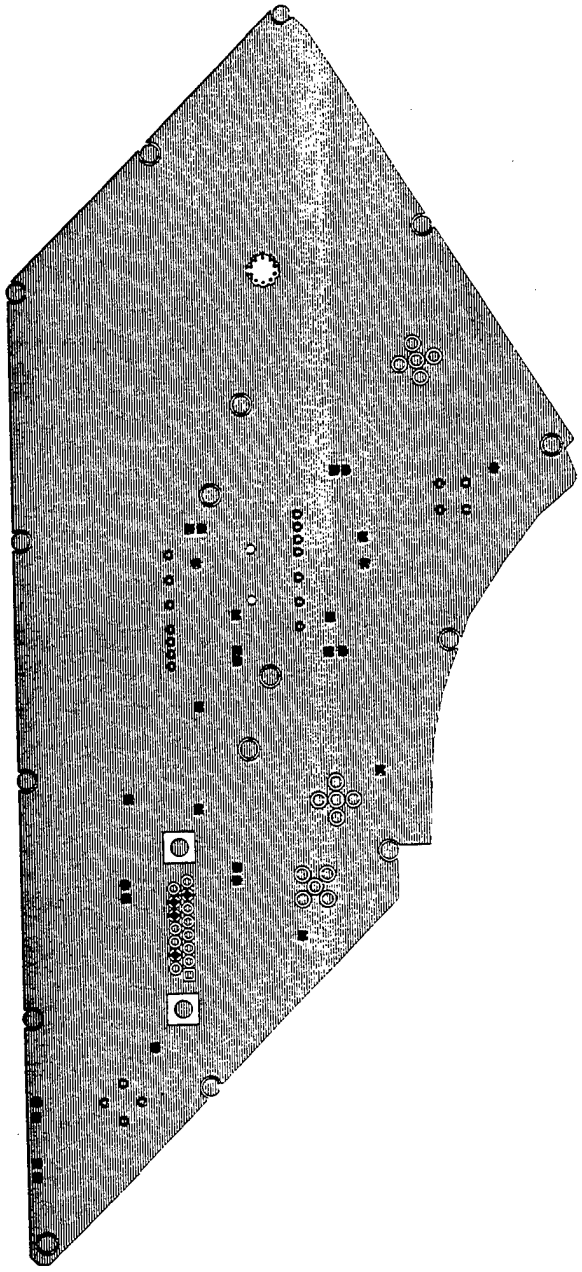


Figure 45 RF HPA PCB - Bottom (ground) Layer Photoplot

APPENDIX D. PRINTED CIRCUIT BOARD DESIGN

This appendix describes printed circuit board design and construction. A glossary of terms associated with PCB's is provided to help the reader understand the text as well as speak intelligently to others in the PCB design field. It assumes the PCB designer will be using a computer aided design (CAD) tool for PCB design.

A. BACKGROUND

A printed circuit board is a wiring structure used for the interconnection of electrical devices. It consists of a thin film of conductive material deposited on a non-conducting planar surface. The electrical devices are mounted to the planar surface with their leads connected by the film of conducting material. This film is typically shaped into lines, called traces. The use of PCB's has allowed the mass production of electrical systems and minimized the space taken by those systems. PCB complexity increases with the number of holes, the number of layers and the size of the PCB.

B. GLOSSARY

1 Oz. Copper - A conducting material used in PCB construction consisting of thin film (1.4 mils thick) of copper. A solid plane of the copper weighs 1 ounce per square inch.

Aperture - A specially shaped hole, used by a photoplotter to pass light through to create a given shape on a film. An aperture can be used without movement to make a shape or with movement to make a line or arc.

Anti-Pad - The area surrounding a pad which is void of all conducting material when a pin is not connected. Typically appears as a "swollen" version of the pad.

Blind Via - A via which does not go all the way through the PCB, just between two or more internal layers and is invisible on the exterior of the PCB. Figure 46 shows a blind via.

Buried Via - A via which goes partially through the PCB and is visible from the exterior of the PCB. Figure 47 shows a buried via.

Dielectric - A non-conducting insulative material used between layers in a PCB.

DRC - Design rule check, a CAD program may have the capability of checking the design database against a set of user defined rules to aid in determining design and manufacturing validity.

Flash - A shape made by a photoplotter when the aperture is not moving.

Footprint - The specific geometry of the pin holes and mounting holes together with the pads necessary for the mounting and connection of an electrical device to a PCB.

G-10 Epoxy - A commonly used epoxy fiberglass dielectric for PCB construction. A low out-gassing material which can be used in space applications. Typical thickness' include

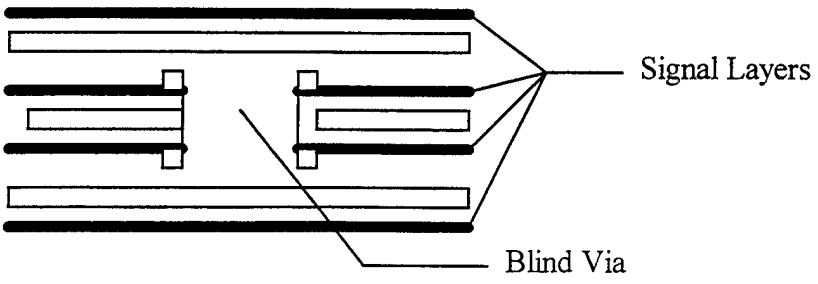


Figure 46 Blind Via

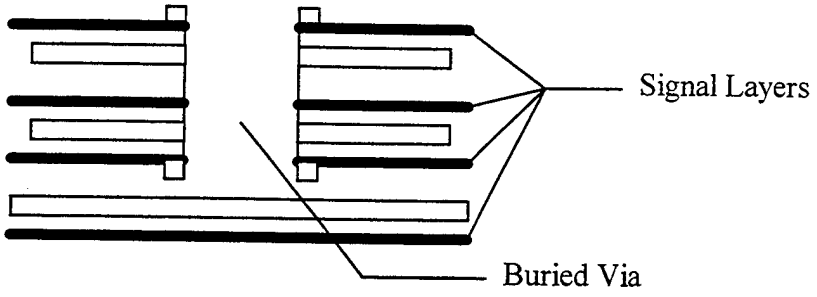


Figure 47 Buried Via

5,10,15,31 and 62 mils.[Ref.6]

FR-4 - A flame retardant version of G-10 Epoxy.

GERBER - A set of standard computer generated data formats used to describe the layers of a PCB for the manufacturer. Name originates from the Gerber Scientific Company, an early pioneer in photoplotter manufacturing. [Ref.7]

Layer - A planar surface of conducting material. Layers can be stacked on top of one another to form a multi-layer PCB.

Layout - Refers to the entire process of PCB design. The process of physically placing component footprints and interconnections on a PCB. Typically done using a CAD tool.

Net - The logical connection between two pins.

Netlist - An ASCII file which contains the interconnection data between integrated circuit pins. A netlist is typically extracted from a schematic drawing by a computer aided design tool.

NC Drill File - An ACSII data file containing the data required to drill the holes in the PCB with a numerically controlled drill. Usually generated by a computer aided design program.

NC Route File - An ASCII data file containing the data required to cut the final exterior shape of the PCB with a numerically controlled router. Usually generated by a computer aided design program, not required for simple PCB exterior geometry.

Pad - The conductive material surrounding the plated-through hole for a pin which allows a connection between the pin and other traces or planes.

Padstack - A multi-layer build-up of pads around a hole for a pin. Specifies which pads will be used in each layer. Figure 48 and Figure 49 show padstack composition.

Plane - A thin film of conducting material which covers a large area of the PCB. Planes are generally used to provide ground and power connections because they provide a low resistance interconnect.

Photoplotter - A plotter that writes using light. Just as in the case of a pen plotter, a photoplotter must be told which tool to use, were to go next and the path to use to the next point. For a photoplotter, a "tool" means an aperture. [Ref.7]

Rats (Nest) - A display by some CAD programs to aid in component placement and routing and can only be used in conjunction with a netlist. The rats nest is a straight line connection of all the nets on a component, allowing the PCB designer to see what connections need to be made when placing the component.

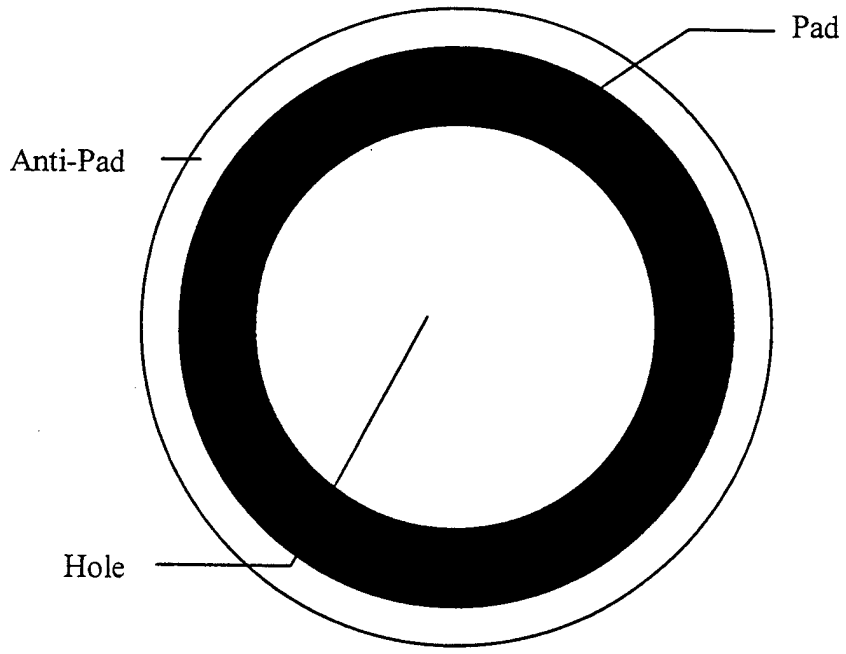


Figure 48 Padstack - Top View

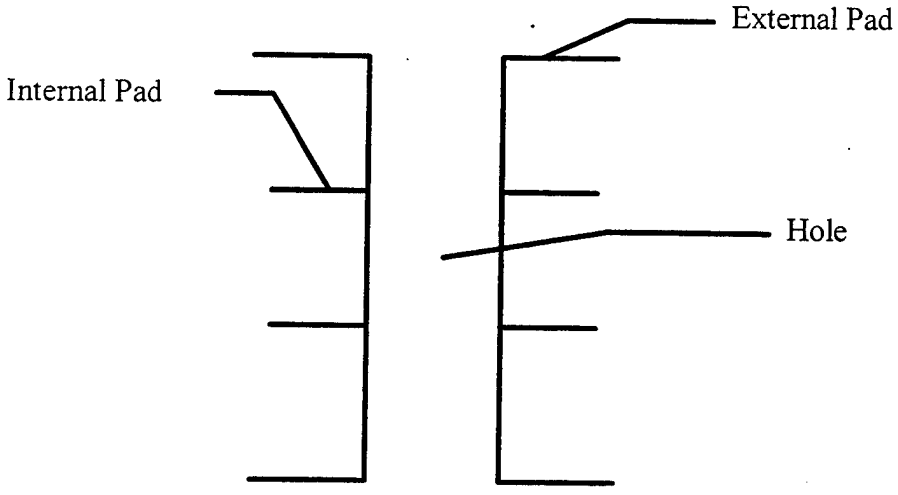


Figure 49 Padstack - Side View

Routing - The process of connecting the pins of components on a PCB to match the connections in a schematic.

RS-274D - An ASCII file of vector GERBER data derived from the traditional numerical control tool languages. Requires a separate aperture list.

RS-274X - An ASCII file of raster GERBER data derived from the traditional laser printer data formats. Does not require a separate aperture list.

Surface Mount - A PCB mounting strategy where the components are placed on the surface of the PCB with no holes drilled through the PCB for mounting. This is a newer technique which allows a higher number of components per PCB because the components can be placed, on opposite sides of the board, above and below one another.

Thermal Relief - A structure placed in a layer around the connection of a pin to a plane to prevent the heat generated from soldering elsewhere on the plane from damaging the component if it were fully connected to the plane. Figure 50 shows a thermal relief.

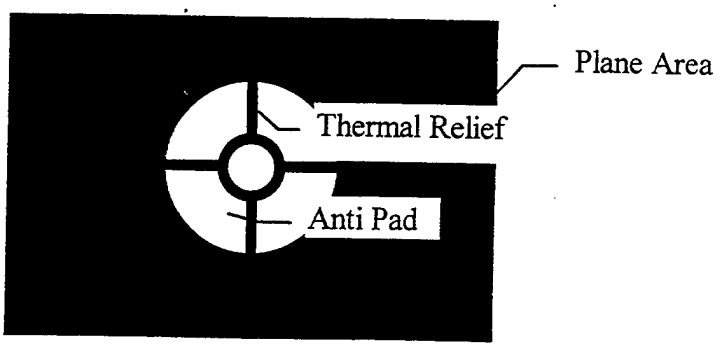


Figure 50 Thermal Relief

Through Mount - A PCB mounting strategy for components where the component leads extend through the PCB. This is an older technique which does not allow components to be placed directly above and below one another.

Trace - A line formed on a PCB, used to connect pins on components replacing a wire.

Via - A hole through a PCB which has been plated through with a conducting material to provide inter-connections between layers of the PCB.

C. BASIC CIRCUIT BORD DESIGN STEPS

The basic steps in PCB design follow. This description is made to be generic and apply to any type of PCB using the commercially available CAD software. Not all CAD software will have all the capabilities discussed below.

1. Footprint Creation

The PCB designer reviews the schematic and the bill of materials and determines all the parts necessary. A review of the manufacturer's data sheets for the components will give the physical component size and pin spacing. The PCB designer then looks in the standard libraries provided with his CAD tool as well as his own previously built libraries for any component footprints which currently exist, comparing these with the components to ensure their applicability.

a. Padstack Creation

When a new footprint must be created, the required padstacks are first created or retrieved from a library. A padstack is created by first determining the physical dimension of the leads on the component. This can be done from the manufacturer's data sheet or physically measuring the leads with a micrometer. This dimension is used to

specify the hole drilled for the component which will form the center of the padstack. Components should fit snugly into the PCB, without the need for force or undue pressure, but not loose enough to fall out when soldered in place. A typical hole might be 4 to 6 mils larger in diameter than the exterior pin diameter[Ref.6].

Pad size is determined by the component packaging type and pin spacing. A pad should be large enough to allow good electrical connection and not interfere with the adjacent pads. Pads must also not short pins to their case. Pads may be different sizes in different layers and need not be circular. The anti-pad is generally a "swelling" of the pad around the hole by 10-45 mils, but need not be the same shape as the pad. A typical technique is to change the anti-pad shape on one pin of a component to allow easy determination of a reference pin on the PCB. A thermal relief may also be associated with the padstack. Many CAD programs allow the creation and storing of padstacks in a library for future use.

For surface mount components, padstack creation is simplified. The pads will only exist on one layer and are typically rectangular. A surface mount pad is typically the same width as the pin on the component and 10-30 mils longer. The anti-pad will extend around the perimeter of the pad. Thermal relief's are not usually generated for surface mount pads because planes are not typically placed around surface mount components.

b. Pin Spacing Layout

When the required padstacks are created, they are placed in the physical geometry of the component, allowing the component to be placed on the PCB. It is critical that the holes for component leads or the surface mount pads match the components exactly. A skewed lead could cause weakening of the lead and premature failure of the component package. At frequencies above 10 Mhz, a skewed lead may cause signal distortion.

A component footprint is typically saved in a library following creation. The footprints are usually named by their package and not the schematic part name because many different components use the same packages and have the same footprints. The prudent PCB layout engineer will print a 1:1 test plot of the created component and check for fit with an actual component. This prevents unnecessary rework after PCB manufacture.

2. Physical PCB Size and Constraints

PCB size is determined by the physical size of the finished product needed to fit in a particular housing. This may be left up to the PCB engineer, at which point a first guess on size should be made. This guess may be made based on knowledge of the PCB designer or by looking at other PCB's of similar complexity. Any other constraints such as connector or mounting hole location must be determined before layout starts, as this will drive component placement.

A CAD system may also allow design constraints and rules to be specified. The default design rules are a good place to start and should be modified only after consulting

with the PCB manufacturer as to the ability for the manufacturer to physically create the design using those rules. Constraints such as route keep-in/out and package keep-in/out may be specified to enhance the use of the CAD tool in creating a correct design the first time.

The number of layers in the PCB should also be specified prior to placing of components and routing. The number of layers will be determined by the component density and routing difficulty, as well as any desire to use a power or ground plane. A typical PCB has 4 layers, a top and bottom for signal routing and a power and ground plane. The PCB should have an even number of layers if possible, especially if it is odd shaped. This allows the manufacturer to build the PCB around a center core of dielectric and will prevent warping of the board in the manufacturing process, as the layers are roll bonded together.

3. Component Placement

Component footprints are placed on the PCB to allow for optimum routing and circuit performance. Some CAD tools have algorithms to aid in placement for optimum routing and will automatically place components. If the CAD program has the ability to import a netlist, this will allow the PCB designer to see component interconnection as he is placing the parts. This is a valuable tool in getting the components in the correct place the first time.

The first components placed should be those with physical constraints requiring them in a specific location on the PCB. Typically connectors and large components will have these constraints. Components with critical signal paths are placed next. This

requires the PCB layout designer to have a good knowledge of the schematic and underlying circuit. The remaining components are placed by placing integrated circuits first, followed by discrete components.

Components must be placed to enhance the "routability" of the board , the operation of the circuit, and the ability to physically make and assemble the board. Components should never be touching or so close that assembly becomes impossible. The novice PCB designer may want to consult an experienced engineer or look at other work which has been done to get a feel for the proper placement of components. Care must be taken near mounting holes, connectors and other structures to keep components an appropriate distance away. The PCB designer should know what type of fasteners are to be used for PCB mounting and their size, particularly head size, before placing components to avoid have a conflict between a screw and a component package.

4. Routing

Routing is the physical interconnection of pins on components with traces and provides the electrical connections necessary to complete the circuit. Use of a "Rats Nest" allows the PCB designer to see connections between pins before they are routed and enhances the ease of routing. Some CAD programs will perform automatic routing when given a proper set of constraints. Connections between pins can be made on the same layer or span multiple layers by using vias.

The first traces routed are the critical signal paths, which should be as short as possible with as few layer changes as possible. All other signals are then routed. Power and ground are provided last. If possible, the use of power and ground planes is desired.

These planes reduce noise and provide low resistance distribution networks. Trace width should be wide enough to carry the current required without overheating. Coombs [Ref.6] provides curves on the current carrying capability of traces.

For high frequency signals, in excess of 10 Mhz, special circuit construction techniques must be used to ensure signal purity. This occurs because the signals are propagating as RF waves through a transmission line. Appendix E discusses these circuit construction techniques.

5. Manufacturing Data Creation

When layout and routing are complete, data files for the PCB manufacturer must be created. The layers are typically described using the GERBER data format. Each layer requires a separate GERBER file. The holes are described using NC drill data, and if the PCB is odd shaped, NC route data should be provided to the manufacturer. CAD programs will create the required data files. The PCB designer should check with the manufacturer as to the particular data file format the manufacturer supports.

All manufacturing data should be checked prior to submission. If possible, a separate CAD program from the one used for design should be used. This will prevent any CAD system biases from entering the data.

APPENDIX E. STRIPLINE AND MICRO STRIP CIRCUIT CONSTRUCTION

This appendix describes basic stripline and micro strip circuit construction. These techniques are used when signal frequency on a PCB is so high (above 10 Mhz) that transmission line techniques must be used to ensure signal purity. Design equations for characteristic impedance of traces are also provided.

A. STRIPLINE CIRCUIT CONSTRUCTION

A stripline transmission line consists of 2 parallel ground planes separated by a dielectric with a signal plane between the ground planes. Figure 51 shows an example of a stripline transmission line. Stripline construction encases the signal within ground planes. This allows the signal to be more immune to noise exterior to the PCB. This construction technique requires the use of through mount components. It does not support surface mount components as the ground plane must remain unbroken.

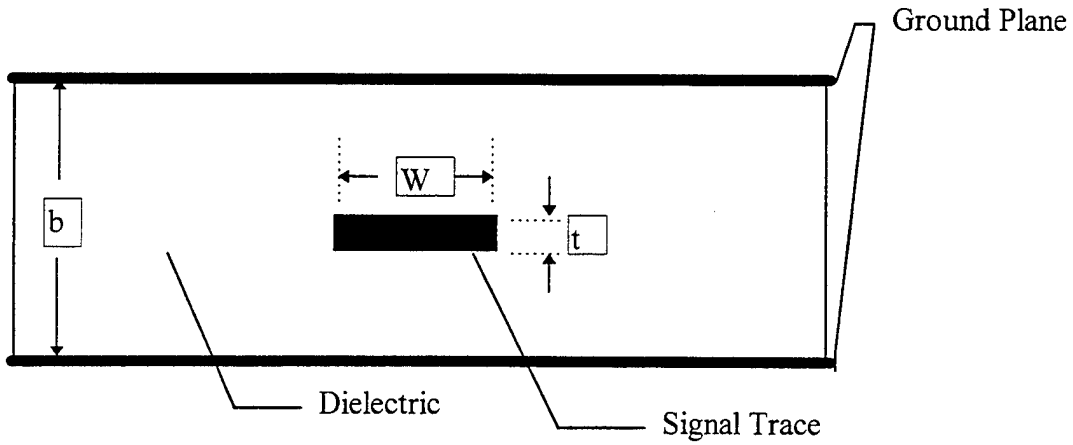


Figure 51 Stripline Transmission Line. After Ref[7].

The most important characteristic of the stripline is its characteristic impedance. When a single stripline is used, the impedance is real and given by the following equation [Ref.8]:

$$Z_o = \frac{94.15}{\left(\frac{\frac{w}{b}}{1-\frac{t}{b}} + \frac{C_f'}{0.0885\varepsilon_R} \right) \sqrt{\varepsilon_R}} \tag{1}$$

Where:

$$C_f' = \frac{0.0885\varepsilon_R}{\pi} \left[\frac{2}{1-\frac{t}{b}} \ln\left(\frac{1}{\left(1-\frac{t}{b}\right)} + 1 \right) - \left(\frac{1}{1-\frac{t}{b}} - 1 \right) \ln\left(\frac{1}{\left(1-\frac{t}{b}\right)^2} - 1 \right) \right] \tag{2}$$

and t, b and w refer to the thickness of the stripline, spacing between ground planes and width of the stripline respectively, as shown in Figure 51. Eqn. 1 applies when the stripline is between equal thickness dielectric and the ratio w/b is greater than 0.35. Solving Eqn.1 for w yields:

$$w = b\left(\frac{94.15}{Z_o\sqrt{\varepsilon_R}} - \frac{C_f'}{0.0885\varepsilon_R} \right)\left(1-\frac{t}{b}\right) \tag{3}$$

Eqn.3 is a more useful form of Eqn.1 because typically the dielectric thickness and conductor thickness is fixed and the designer is left with the stripline width to control characteristic impedance.

When a stripline is required to change directions on a PCB, the designer must make sure the impedance of the stripline remains matched at the operating frequencies to prevent a high return loss. A 90 degree right angle bend is mismatched at all frequencies [Ref.8]. The match is best made with a mitered 90 degree corner or a small bend. Howe [Ref.8] presents experimental data showing the effects of various bends on matching in a stripline. The recommended technique for tight bends is the 90 degree mitered corner. For area where there is more room, a curve with a radius of 3 line widths or greater is recommended. A curve with this radius has almost no difference in impedance compared to a straight line.

When striplines are run in parallel on a PCB, they capacitively couple to each other. This is the principle used in the design of stripline filters, couplers and transformers. This is not desired when designing with discrete components. Capactive coupling is prevented by not running high frequency striplines in parallel on a PCB. When the traces must be physically close, such as entering a component, they should approach from 90 degree angles.

B. MICROSTRIP CIRCUT CONSTRUCTION

A micro strip transmission line consists of a conductor placed over a ground plane separated by a dielectric material. Figure 52 shows a micro strip transmission line structure. A microstrip circuit has no upper ground plane, requiring more careful shielding for the top of the PCB to prevent EMI.

As with the stripline transmission line, the micro strip line characteristic impedance is critical. The electromagnetic fields surrounding the micro strip structure

differ from the stripline because of the lack of the upper ground plane. The following equation describes the micro strip characteristic impedance [Ref.9]:

$$Z_o = \frac{\frac{120\pi}{\sqrt{\varepsilon_{ff}}}}{\frac{W}{h} + 1.393 + 0.667 \ln\left(\frac{W}{h} + 1.444\right)} \tag{4}$$

where

$$\varepsilon_{ff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left(1 + 12\frac{h}{W}\right)^{-\frac{1}{2}} \tag{5}$$

and h and W refer to the dimensions given in Figure 52.

The following equations [Ref.9] are used in design for selecting the width of the micro strip line:

$$W = h\frac{8e^A}{e^{2A} - 2} \tag{6}$$

where

$$A = \frac{Z_o}{60}\sqrt{\frac{\varepsilon_r + 1}{2}} + \frac{\varepsilon_r - 1}{\varepsilon_r + 1}\left(0.23 + \frac{0.11}{\varepsilon_r}\right) \tag{7}$$

The same construction techniques which apply to stripline circuits also apply to micro strip circuits. The mounting on PCB's containing micro strip transmission lines is more critical because of the exposed fields above the PCB. The PCB should be mounted in a metal box with a shielded metal lid.

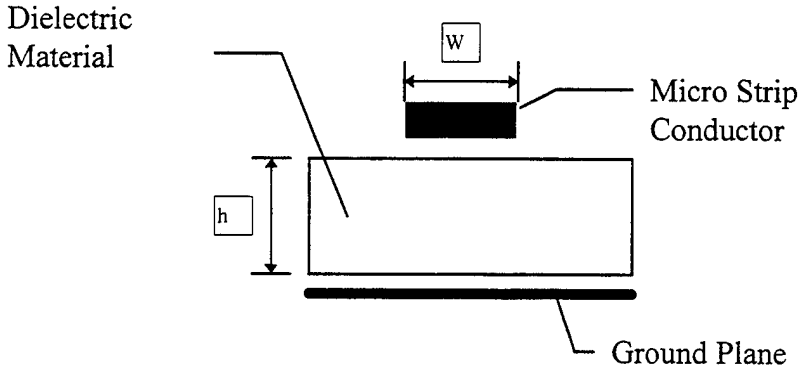


Figure 52 Micro Strip Transmission Line

APPENDIX F. LINK BUDGET ANALYSIS

This appendix contains a derivation of the link analysis for the Petite Amateur Navy Satellite (PANSAT). The derivation starts with the general satellite link equations from Ha [Ref.10], and reduces them to a set of PANSAT specific equations. The actual component values are then substituted into the equations and the link margin is determined. The worst case values are used for all data to provide an estimate of the worst case link margin.

A. DATA LINK BIT ERROR PROBABILITY

A link analysis is a power budget used to determine signal to noise ratio at various points in the satellite link. The required performance for the PANSAT data link specifies a probability of bit error (P_b) of 10^{-5} for the data link. PANSAT is a regenerative satellite repeater because it demodulates the digital data prior to retransmission. The P_b for a regenerative repeater is given by Sklar [Ref.11]:

$$P_b = P_u + P_d - 2P_uP_d \tag{8}$$

Where P_u is the probability of bit error for the up link and P_d is the probability of bit error for the down link. PANSAT uses the same frequency for both the up link and down link, and the users can be assumed to be at the maximum usable range from the satellite in similar weather conditions. This allows the assumption that P_u and P_d are equal. Therefore Equation (8) becomes:

$$P_b = 2P_B - 2\left(P_B\right)^2 \tag{9}$$

Where $P_B = P_u = P_d$. Substituting $P_b=10^{-5}$ into Equation (9) yields $P_B= 5(10^{-6})$.

B. ENERGY PER BIT TO NOISE POWER SPECTRAL DENSITY

The use of direct sequence spread spectrum has no effect on the probability of bit error for coherently detected differentially encoded binary phase shift keying in the presence of additive gaussian white noise [Ref.12]. Therefore the probability of bit error is the same as without spreading and is given by Sklar [Ref.11]:

$$P_B = 2Q\left(\sqrt{\frac{2E_b}{N_o}}\right)\left[1-Q\left(\sqrt{\frac{2E_b}{N_o}}\right)\right] \qquad \textbf{(10)}$$

Where $\left(\frac{E_b}{N_o}\right)$ is the dimensionless ratio of energy per bit to noise power spectral density.

Substituting $P_B= 5(10^{-6})$ into Equation (10) yields $\left(\frac{E_b}{N_o}\right) = 10.425 = 10.181 \quad dB$

C. LINK ANALYSIS EQUATIONS

The basic link equations for the up link and down link are taken from Ha [Ref.10]:

$$\left(\frac{C}{N}\right)_U = EIRP_{SAT} - 20\log\left(\frac{4\pi f_u d_u}{c}\right) + \frac{G_u}{T_u} - 10\log(k) - 10\log(B) - BO_i - L \qquad \textbf{(11)}$$

$$\left(\frac{C}{N}\right)_D = EIRP_{S,SAT} - 20\log\left(\frac{4\pi f_d d_d}{c}\right) + \frac{G}{T} - 10\log(k) - 10\log(B) - BO_i - L' \qquad \textbf{(12)}$$

Where:

U,u indicates term pertains to the up link
D,d indicates term pertains to the down link.
$\left(\frac{C}{N}\right)$ = Carrier to noise ratio (dB).

$EIRP_{SAT}$ = Carrier effective isotropic radiated power (EIRP) to saturate traveling wave tube amplifier at ground station (dBW).

f = Carrier frequency (Hz).

d = Slant range distance to satellite (m).

c = Speed of light, 2.99792458 m/s.

G_u = Satellite antenna gain.

T_u = Satellite system noise temperature (K).

G = Ground station antenna gain.

T = Ground station noise temperature.

k = Boltzmann's constant, $1.380658(10^{-23})$ J/K.

B = Noise bandwidth of satellite channel (Hz).

BO_i,BO_o = Required traveling wave tube amplifier back off (dB).

L = Sum of antenna tracking loss and atmospheric attenuation for up link (dB).

L' = Sum of antenna tracking loss and atmospheric attenuation for down link (dB).

The general link equations are modified for use in the PANSAT link budget. PANSAT uses transistor amplifiers in both the ground station and the satellite, so the back off terms, BO_i and BO_o, are not required. The dependence of the EIRP terms on traveling wave tube amplifier saturation may also be removed because of the transistor amplifiers in the satellite and ground station. The up link and down link frequencies are the same, 436.5 MHz. PANSAT is capable of either transmitting or receiving, but not both at the same time. Therefore the distance to the satellite and the atmospheric attenuation and antenna loss will be the same for the up link and down link.

The modified satellite link equations are given below. Where S indicates a parameter on the satellite and G indicates a parameter on the ground station.

$$\left(\frac{C}{N}\right)_U = EIRP_G - 20\log\left(\frac{4\pi fd}{c}\right) + \frac{G_S}{T_S} - 10\log(k) - 10\log(B) - L \qquad \textbf{(13)}$$

$$\left(\frac{C}{N}\right)_D = EIRP_S - 20\log\left(\frac{4\pi fd}{c}\right) + \frac{G_G}{T_G} - 10\log(k) - 10\log(B) - L \qquad \textbf{(14)}$$

The following equation can be used to convert carrier to noise ratio, to energy per bit noise density ratio [Ref.10]:

$$\frac{E_b}{N_o} = T_b B\left(\frac{C}{N}\right) \tag{15}$$

Where T_b is the bit duration in seconds. Expressing Equation (15) in decibels yields:

$$\frac{E_b}{N_o} = 10\log(T_b) + 10\log(B) + \left(\frac{C}{N}\right)(db) \tag{16}$$

Substituting Equation (16) into Equation (13) and Equation (14) yields the final link equations.

$$\left(\frac{E_b}{N_o}\right)_U = EIRP_G - 20\log\left(\frac{4\pi fd}{c}\right) + \frac{G_S}{T_S} - 10\log(k) - L + 10\log(T_b) \tag{17}$$

$$\left(\frac{E_b}{N_o}\right)_D = EIRP_S - 20\log\left(\frac{4\pi fd}{c}\right) + \frac{G_G}{T_G} - 10\log(k) - L + 10\log(T_b) \tag{18}$$

D. FREE SPACE LOSS

Free space loss is the attenuation in the signal between the satellite and the ground station caused by the propagation of the electromagnetic wave through space over the distance of the link. Free space loss is represented by the term $-20\log\left(\frac{4\pi fd}{c}\right)$ in the link equations.

The slant range to the satellite can be determined by the following equation [Ref.10]:

$$d = \sqrt{\left(R_e + H\right)^2 + R_e^2 - 2R_e\left(R_e + H\right)\sin\left[E + \sin^{-1}\left(\frac{R_e}{R_e + H}\cos(E)\right)\right]} \tag{19}$$

E = elevation angle to satellite in degrees.

The height above the earth's surface for PANSAT is determined by the launch platform and launch mission. PANSAT is expected to be launched from the Space Shuttle at a maximum height of 408 kilometers (408000 meters). The minimum usable elevation angle is 10 degrees. Substituting these values into Equation (19), yields d = 1461047.1 meters. Using the up link and down link frequency of 436.5 MHz and the above distance, the free space loss is 148.45 dB.

E. RECEIVER SENSITIVITY

Receiver sensitivity $\left(\frac{G}{T}\right)$ is the ratio of antenna gain to system noise temperature. Gain is a dimensionless number and temperature is expressed in degrees Kelvin (K). The ratio is normally expressed in decibels. The system noise temperatures are calculated for all components up to the 70 MHz intermediate frequency (IF) input to the modem. The IF section will be separately tuned based on the signal to noise ratio available at the input to the modem. This differs from most link analyses which use all components up to the demodulator input.

1. Ground Station Receiver Sensitivity

The ground station in this analysis is the station at the Naval Postgraduate School which will serve as the controlling station for the satellite. This ground station contains a very high gain antenna and powerful amplifier.

a. Antenna Gain

a. Antenna Gain

The ground station antenna is a KLM 435-40CX high gain circular polarized antenna. The gain (G) on the main axis is 15.2 dB and the antenna is equipped with a computer driven tracking system to keep the main axis pointed to the satellite.

b. Antenna Noise Temperature

Antenna noise temperature has contributions from "spillover of radiation, blockage, and, in general, various inefficiencies" [Ref.12]. The antenna noise temperature can be determined from the following equation [Ref.12]:

$$T_{AC} = K_1 T_S + K_2 T_S + K_2 T_g \tag{20}$$

Where:

T_{AC} = antenna noise temperature for a clear sky (K).
T_S = sky noise temperature under clear conditions (K).
T_g = ground temperature (K).
K_1 = efficiency of antenna main beam.

$$K_2 = \frac{1 - K_1}{2}$$

The ground station antenna efficiency (K_1) is 0.75. Fthenakis [Ref.12] assumes that "half of the spurious radiation is directed to the sky and half to the ground". This allows T_g to be approximated as $T_g = T_o = 290K$ [Ref.12], where T_o is the ambient temperature. T_s is obtained from Fthenakis [Ref.12] for a frequency of 436.5 MHz and an elevation angle of 10 degrees, $T_s = 6.5$ K. Substituting into Equation (20) yields $T_{AC} =$ 41.94 K.

Equation (20) is for clear sky conditions. Rain has the effect of raising the system noise temperature and this is accounted for in the antenna noise temperature calculation.

Ha [Ref.10] states that rain attenuation is only a problem at frequencies above 10 GHz. PANSAT will operate at 436.5 MHz. The rain models, such as the Crane model, for predicting rain attenuation are not accurate below 10 MHz. Due to the unavailability of data, rain attenuation in this calculation will be assumed to be 1 dB. Total antenna noise temperature is given by the following [Ref.12]:

$$T_A = T_{AC} + \left(\frac{1 - L_R}{L_R}\right) T_O \tag{21}$$

Where T_A is total antenna noise temperature and L_R is loss due to rain. Substituting T_{AC} and L_R = 1 dB into Eqn. A.14 yields T_A = 101.6 K.

c. Composite Receiver Noise Temperature

Sklar expresses the composite receiver noise temperature of a receiver having *n* stages as [Ref.11]:

$$T_{comp}^o = T_1^o + \frac{T_2^o}{G_1} + \frac{T_3^o}{G_1 G_2} + \cdots + \frac{T_n^o}{G_1 G_2 \cdots G_{n-1}} \tag{22}$$

Where T_n^o is the effective noise temperature of stage *n* in the receiver network and G_n is the gain in stage *n* of the receiver network. The gain, G, of a loss stage is considered to be $\frac{1}{L}$ where L is the loss of the stage. For a lossy line in the network, $T^o = (L-1)290$ [Ref.11]. For an amplifier stage, $T^o = (F-1)290$ [Ref.11], where F is the noise figure of the amplifier. Table 9 shows the contribution of the ground station components to the composite receiver noise temperature in Equation (22). Adding the contributions of the ground station components yields T_{comp}^o = 135.58 K.

Receiver Component	L (dB)	G (dB)	F (dB)	Stage Noise Temp (K)	Contribution to Tcomp (K)
5 Feet Coaxial Cable	0.1			8.812	8.812
Landwehr Preamplifier		16.0	1.1	83.592	86.132
20 Feet Coaxial Cable	0.5			36.887	0.955
K+L Bandpass Filter	5.0			627.061	18.294
Avantec UTC-517 Amp		22.0	2.5	225.701	20.823
Mini-Ckts ZFM-1W Mixer	5.4		6.4	975.896	0.568

Table 9 Ground Station Component Contribution to System Noise Temperature

d. System Noise Temperature

The total system noise temperature of the ground station is given by the following equation from Sklar [Ref.11]:

$$T_S^o = T_A^o + T_{comp}^o \tag{23}$$

Substituting antenna and composite noise temperature into Equation (23) yields $T_S^0 =$ 237.18 K. Calculating receiver sensitivity for the ground station yields $\left(\frac{G_G}{T_G}\right)$ = -8.55 dB.

2. Satellite Receiver Sensativity

a. Antenna Noise Temperature

The Satellite antenna gain is -2.7 dB at the worst null. This value is used because PANSAT is a free tumbling satellite and no specific point of the antenna pattern will be pointing to the earth at any given time.

b. Antenna Noise Temperature

Antenna noise temperature is 300 K. This is based on the satellite having a nearly omni-directional antenna and receiving noise from the sun, earth and other galactic sources.

c. *Composite Receiver Noise Temperature*

Using Equation (22), the composite receiver noise temperature is calculated. Table 10 shows the contribution of the various components of the satellite receiver to the noise temperature. Adding the contributions of the ground station components yields $T^{o}_{comp} = 2890.95$ K.

d. *System Noise Temperature*

Substituting antenna and composite noise temperature into Equation (23) yields $T^{0}_{S} = 3190.94$ K. Calculating receiver sensitivity for the ground station yields $\left(\frac{G_G}{T_G}\right) = -37.74$ dB.

Receiver Component	L (dB)	G (dB)	F (dB)	Stage Noise Temp (K)	Contribution to Tcomp (K)
Impedance Matching Network	1			75.088	75.088
Band Pass Filter	5			627.061	789.422
RF-300 Relay	0.05			3.358	13.369
TOSW-230 Pin Diode Switch	1.3			101.199	407.547
Avantec UTC-554 Amp		28	3	288.626	1567.962
TOSW-425 Pin Diode Switch	1.1			83.592	0.720
TOSW-230 Pin Diode Switch	1.3			101.199	1.122
SRA-1 Mixer	5.1		6.1	891.403	13.337
PIF-70 Bandpass Filter	0.24			16.477	0.798
TOSW-230 Pin Diode Switch	1.3			101.199	5.178
TOSW-230 Pin Diode Switch	1.3			101.199	6.985
TOSW-230 Pin Diode Switch	1.3			101.199	9.423

Table 10 Satellite Component Contribution to System Noise Temperature

F. EFFECTIVE ISOTROPIC RADIATED POWER

The effective isotropic radiated power (EIRP) is the product of the antenna gain and transmitted power as shown in the following equation [Ref.11]:

$$EIRP = P_t G_t \tag{24}$$

Where P_t is the transmitted power measured at the input to the antenna and G_t is the antenna gain. This means the power out of the amplifiers must be reduced by any losses between the amplifier and the antenna.

1. Ground Station EIRP

The peak output power from the ground station amplifier is 60 W (47.78 dBm). The output power is reduced by 5.6 dB circuit loss, resulting in 42.18 dBm output. The antenna gain is 15.2 dB. Therefore $EIRP_G = 57.38$ dBm.

2. Satellite EIRP

The peak output power from the satellite amplifier is 5 W (37 dBm). The output power is reduced by 7.35 dB circuit loss, resulting in 29.65 dBm output. The antenna gain is -2.7 dB. Therefore $EIRP_S = 26.95$ dBm.

G. LINK MARGIN

The link margin is the excess power available in the satellite link beyond the amount required to close the link. The link margin may be calculated by using Equation (17) and Equation (18):

$$MARGIN_U = EIRP_G - 20\log\left(\frac{4\pi fd}{c}\right) + \frac{G_S}{T_S} - 10\log(k) - L + 10\log(T_b) - \left(\frac{E_b}{N_o}\right)_U \quad \textbf{(25)}$$

$$MARGIN_D = EIRP_S - 20\log\left(\frac{4\pi fd}{c}\right) + \frac{G_G}{T_G} - 10\log(k) - L + 10\log(T_b) - \left(\frac{E_b}{N_o}\right)_D \quad \textbf{(26)}$$

The data rate for the spread mode of communication is 9600 bits/sec. The satellite also contains a narrow band, non-spread mode for maintenance of 78125 bits/sec. The higher data rate will be used in the calculations to be more conservative. This yields a T_b of $12.8(10^{-6})$ seconds. Additional losses (L) will be assumed to be 1 dB. Table 11 shows the contributions to the link margin in Equation (25) and Equation(26).

Component	Uplink	Downlink
EIRP (dBm)	57.38	26.95
Free Space Loss (dB)	148.45	148.45
Receiver Sensitivity (dB/K)	-37.74	-8.55
Boltzman Constant (dBm/K-Hz)	-198.60	-198.60
Additional Losses (dB)	1.00	1.00
Bit Duration (dB-sec)	-48.92	-48.92
(Eb/No) Required	10.18	10.18
LINK MARGIN (dB)	9.69	8.45

Table 11 Link Margin

LIST OF REFERENCES

1. International Telecommunication Union. Radiocommunication Bureau. Weekly Circular 1960/22.01.91. Special Section AR11/A/676. Satellite Network PANSAT. As amended in Weekly Circular 2212/30.01.1996. Special Section AR11/A/676 MOD-1.

2. Brown, A.O. III, *Communications Subsystem for the Petite Amateur Navy Satellite,* Master's Thesis, Naval Postgraduate School, Monterey, CA, September 1993.

3. Dawson, David and Eagle, Pete, "Redesign of the PANSAT RF Subsystem," EC-2990 Design Project, Naval Postgraduate School, Monterey, CA, September 1994.

4. Gerkhe, Olaf, *Design and Analysis of the Housing of the Communication Payload of the Petite Navy Amateur Satellite (PANSAT)*, Master's Thesis, Naval Postgraduate School, Monterey, CA, September 1995.

5. Motorola. *RF Device Data.* Motorola Incorporated, 1996.

6. Coombs, Clyde F., *Printed Circuits Handbook*, McGraw-Hill Book Co., New York, 1979.

7. Alberta Printed Circuits Co., *Basic Photoplotting Principles,* World Wide Web Page, URL: http://www.apcircuits.com/grdef.htm, September 1996.

8. Howe, Harlan, Jr., *Stripline Circuit Design,* Artech House, Inc. Norwood, MA, 1974.

9. Gonzalez, Guillermo, *Microwave Transistor Amplifiers, Analysis and Design,* Prentice Hall, Englewood Cliffs, NJ, 1984.

10. Ha, Tri T., *Digital Satellite Communications*, McGraw-Hill Inc., New York, NY, 1990.

11. Sklar, B., *Digital Communications Fundamentals and Applications,* Prentice Hall, Englewood Clifs, NJ, 1988.

12. Fthenakis, E., *Manual of Satellite Communications*, McGraw Hill, Inc., New York, NY, 1988.

INITIAL DISTRIBUTATION LIST

No. of copies

1. Defense Technical Information Center 2
   8725 John J. Kingman Rd., Ste. 0944
   Ft. Belvoir, VA 22060-6218

2. Dudley Knox Library 2
   Naval Postgraduate School
   411 Dyer Rd.
   Monterey, CA 93943-5101

3. Chairman, Code EC 1
   Department of Electrical and Computer Engineering
   Naval Postgraduate School
   Monterey, CA 93943-5121

4. Prof. Randy L. Borchardt, Code EC/Bt 2
   Department of Electrical and Computer Engineering
   Naval Postgraduate School
   Monterey, CA 93943-5121

5. Prof. Rudolf Panholzer Code 07 1
   Dean of Engineering and Computational Science
   Naval Postgraduate School
   Monterey, CA 93943-5003

6. Chairman, Code SP 1
   Space Systems Academic Group
   Naval Postgraduate School
   Monterey, CA 93943-5110

7. Mr. David Rigmaiden , Code SP/Rd 2
   Space Systems Academic Group
   Naval Postgraduate School
   Monterey, CA 93943-5110

8. LT Carl A. Lahti, USN 1
   30 Teal Lane
   Groton, CT 06340